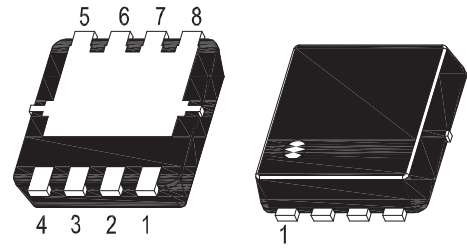
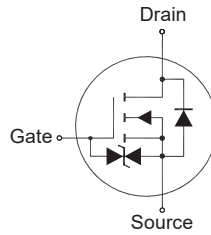


N-Channel Enhancement Mode MOSFET

Features

- Low $R_{DS(ON)}$
- Halogen and Antimony Free(HAF), RoHS compliant
- Built-in G-S Protection Diode
- Typical ESD Protection HBM Class 2



1. Source 2. Source 3. Source 4. Gate
5. Drain 6. Drain 7. Drain 8. Drain
DFN3030 Plastic Package

Classification	Voltage Range(V)
0A	< 125
0B	125 to < 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	≥ 8000

Key Parameters

Parameter	Value	Unit
BV_{DSS}	65	V
$R_{DS(ON)} \text{ Max}$	6.1 @ $V_{GS} = 10 \text{ V}$	m Ω
	10 @ $V_{GS} = 4.5 \text{ V}$	
$V_{GS(th)} \text{ typ}$	1.7	V
$Q_g \text{ typ}$	31 @ $V_{GS} = 10 \text{ V}$	nC

Application

- Motor/Body Load Control
- High Frequency Switching and Synchronous Rectification

Absolute Maximum Ratings (at $T_a = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $T_c = 25^\circ\text{C}$ $T_c = 100^\circ\text{C}$	I_D	50 32	A
Peak Drain Current, Pulsed ¹⁾	I_{DM}	300	A
Avalanche Current	I_{AS}	9.1	A
Single Pulse Avalanche Energy ²⁾	E_{AS}	4.1	mJ
Power Dissipation $T_c = 25^\circ\text{C}$	P_D	25	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	5	$^\circ\text{C/W}$
Thermal Resistance from Junction to Ambient ³⁾	$R_{\theta JA}$	50	$^\circ\text{C/W}$

¹⁾ Pulse Test: Pulse Width $\leq 100 \mu\text{s}$, Duty Cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.

²⁾ Limited by $T_{J(MAX)}$, starting $T_J = 25^\circ\text{C}$, $L = 0.1 \text{ mH}$, $R_g = 25 \Omega$, $I_{AS} = 9.1 \text{ A}$, $V_{GS} = 10 \text{ V}$.

³⁾ For mounting on a PCB, the thermal resistance $R_{\theta JA}$ is determined by the PCB layout and the mounting method.

Characteristics at $T_a = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at $I_D = 250\ \mu\text{A}$	BV_{DSS}	65	-	-	V
Drain-Source Leakage Current at $V_{DS} = 65\ \text{V}$	I_{DSS}	-	-	1	μA
Gate Leakage Current at $V_{GS} = \pm 20\ \text{V}$	I_{GSS}	-	-	± 10	μA
Gate-Source Threshold Voltage at $V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	$V_{GS(th)}$	1.2	-	2.5	V
Drain-Source On-State Resistance at $V_{GS} = 10\ \text{V}$, $I_D = 20\ \text{A}$ at $V_{GS} = 4.5\ \text{V}$, $I_D = 10\ \text{A}$	$R_{DS(on)}$	- -	4.7 -	6.1 10	$\text{m}\Omega$
DYNAMIC PARAMETERS					
Forward Transconductance at $V_{DS} = 5\ \text{V}$, $I_D = 20\ \text{A}$	g_{fs}	-	34	-	S
Gate resistance at $V_{GS} = 0\ \text{V}$, $V_{DS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	R_g	-	1	-	Ω
Input Capacitance at $V_{GS} = 0\ \text{V}$, $V_{DS} = 30\ \text{V}$, $f = 1\ \text{MHz}$	C_{iss}	-	1691	-	pF
Output Capacitance at $V_{GS} = 0\ \text{V}$, $V_{DS} = 30\ \text{V}$, $f = 1\ \text{MHz}$	C_{oss}	-	604	-	pF
Reverse Transfer Capacitance at $V_{GS} = 0\ \text{V}$, $V_{DS} = 30\ \text{V}$, $f = 1\ \text{MHz}$	C_{rss}	-	37	-	pF
Gate charge total at $V_{GS} = 10\ \text{V}$, $V_{DS} = 30\ \text{V}$, $I_D = 20\ \text{A}$ at $V_{GS} = 4.5\ \text{V}$, $V_{DS} = 30\ \text{V}$, $I_D = 20\ \text{A}$	Q_g	- -	31 16	- -	nC
Gate to Source Charge at $V_{GS} = 10\ \text{V}$, $V_{DS} = 30\ \text{V}$, $I_D = 20\ \text{A}$	Q_{gs}	-	5.8	-	nC
Gate to Drain Charge at $V_{GS} = 10\ \text{V}$, $V_{DS} = 30\ \text{V}$, $I_D = 20\ \text{A}$	Q_{gd}	-	7.5	-	nC
Turn-On Delay Time at $V_{GS} = 10\ \text{V}$, $V_{DS} = 30\ \text{V}$, $I_D = 20\ \text{A}$, $R_g = 3.3\ \Omega$	$t_{d(on)}$	-	14	-	ns
Turn-On Rise Time at $V_{GS} = 10\ \text{V}$, $V_{DS} = 30\ \text{V}$, $I_D = 20\ \text{A}$, $R_g = 3.3\ \Omega$	t_r	-	25	-	ns
Turn-Off Delay Time at $V_{GS} = 10\ \text{V}$, $V_{DS} = 30\ \text{V}$, $I_D = 20\ \text{A}$, $R_g = 3.3\ \Omega$	$t_{d(off)}$	-	13	-	ns
Turn-Off Fall Time at $V_{GS} = 10\ \text{V}$, $V_{DS} = 30\ \text{V}$, $I_D = 20\ \text{A}$, $R_g = 3.3\ \Omega$	t_f	-	3	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at $I_S = 1\ \text{A}$, $V_{GS} = 0\ \text{V}$	V_{SD}	-	-	1.3	V
Body-Diode Continuous Current	I_S	-	-	50	A
Body-Diode Continuous Current, Pulsed	I_{SM}	-	-	300	A
Body Diode Reverse Recovery Time at $I_S = 20\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	t_{rr}	-	19	-	ns
Body Diode Reverse Recovery Charge at $I_S = 20\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	Q_{rr}	-	8	-	nC

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

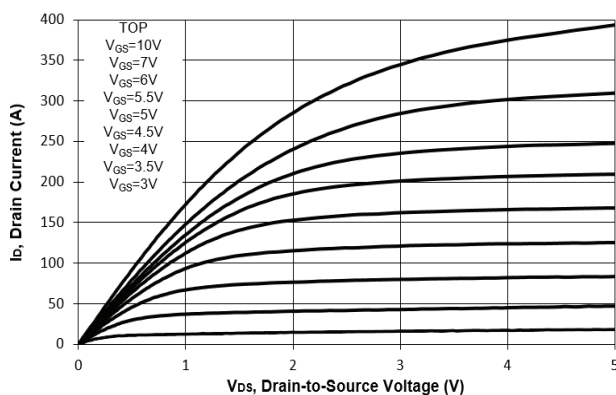


Fig. 2 Typical Transfer Characteristics

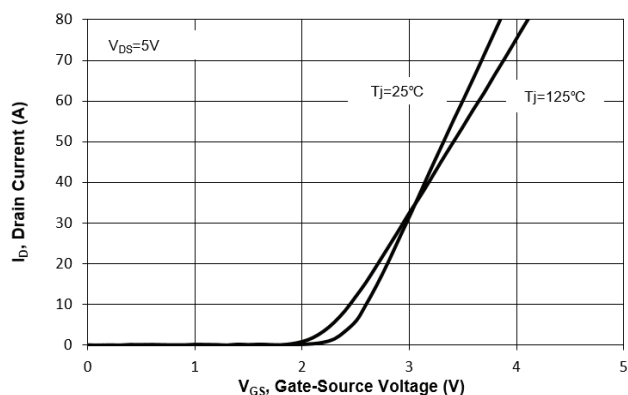


Fig. 3 on-Resistance vs Drain Current

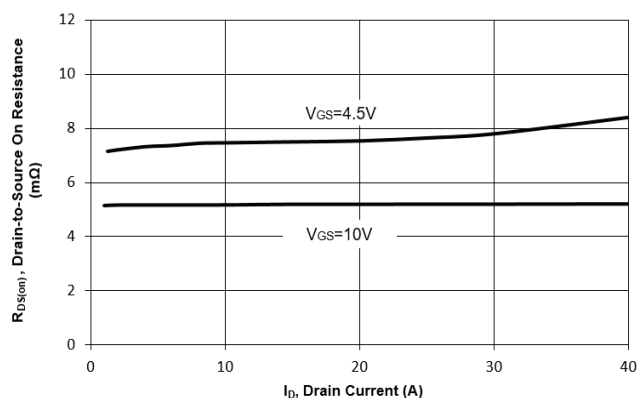


Fig. 4 on-Resistance vs. Gate to Source Voltage

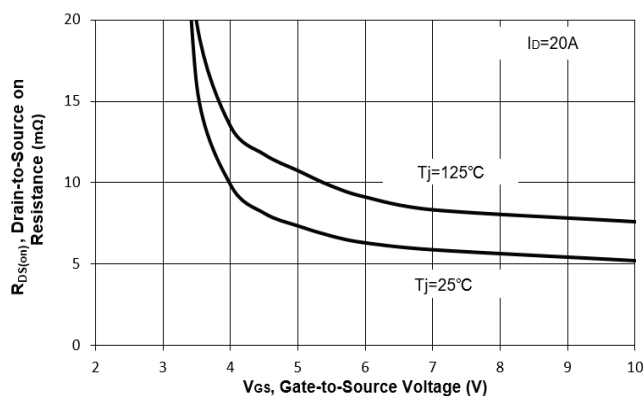


Fig. 5 on-Resistance vs. TJ

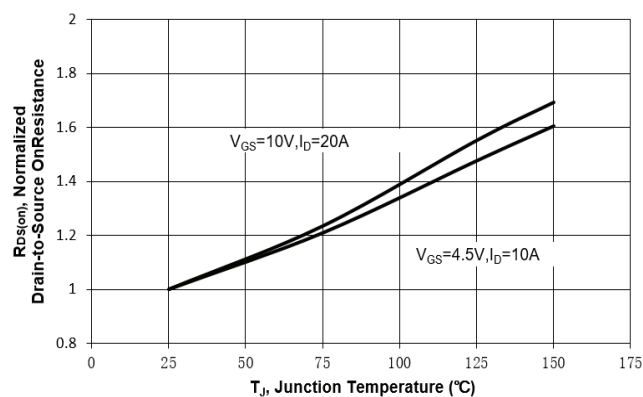
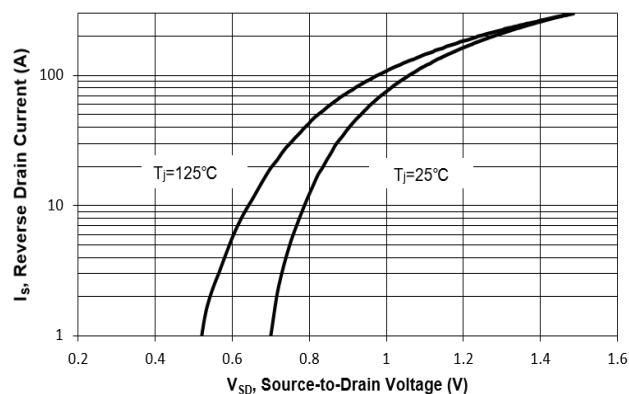


Fig. 6 Typical Body-Diode Forward Characteristics



Electrical Characteristics Curves

Fig.13 Normalized Maximum Transient Thermal Impedance($Z_{\theta JC}$)

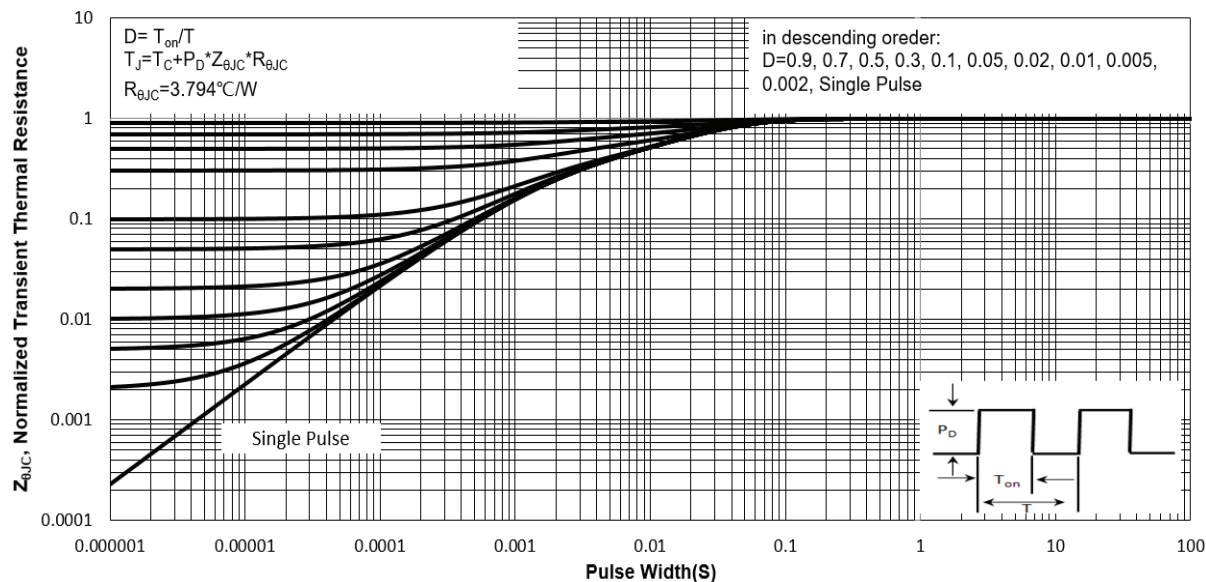
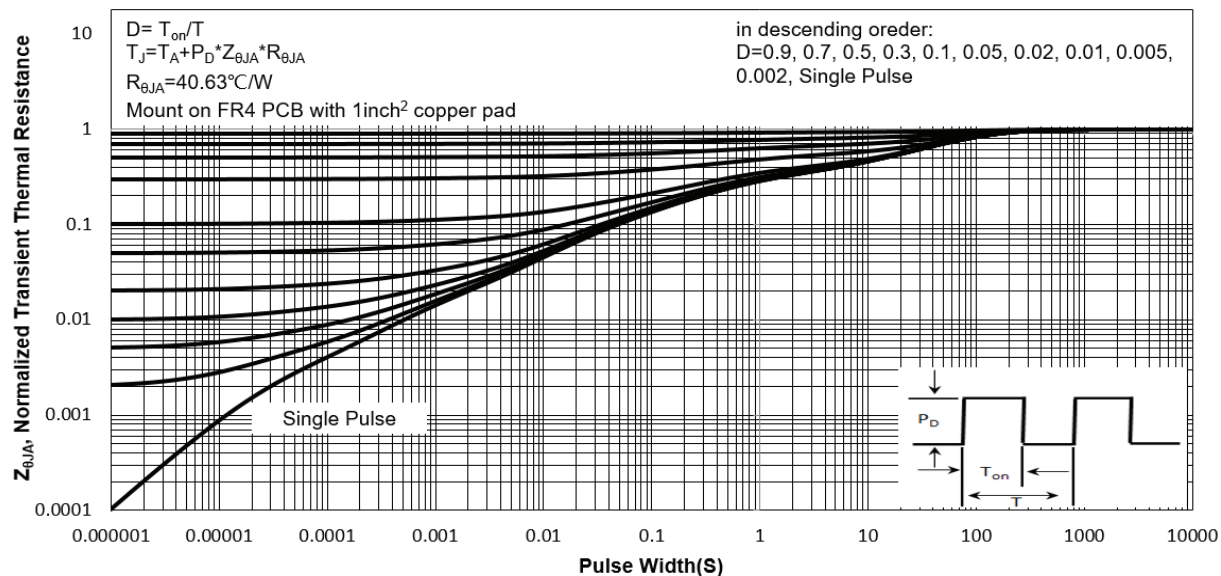


Fig.14 Normalized Maximum Transient Thermal Impedance($Z_{\theta JA}$)



Test Circuits

Fig.1-1 Switching times test circuit

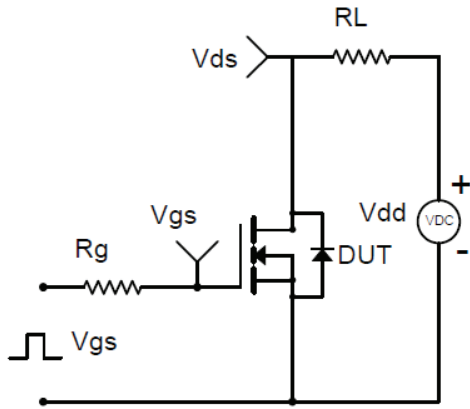


Fig.1-2 Switching Waveform

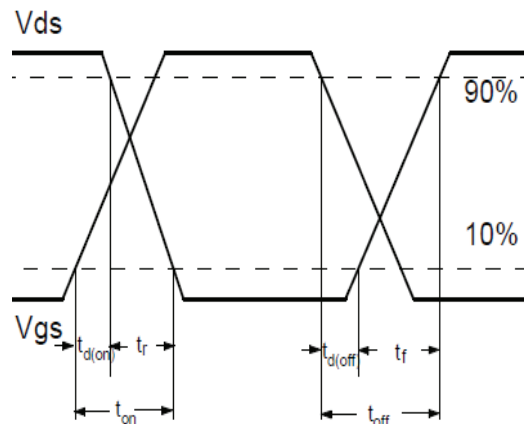


Fig.2-1 Gate charge test circuit

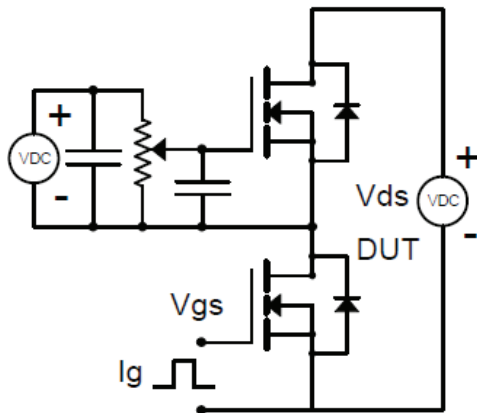


Fig.2-2 Gate charge waveform

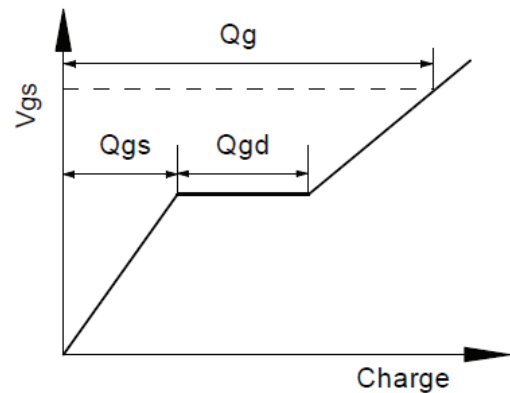


Fig.3-1 Avalanche test circuit

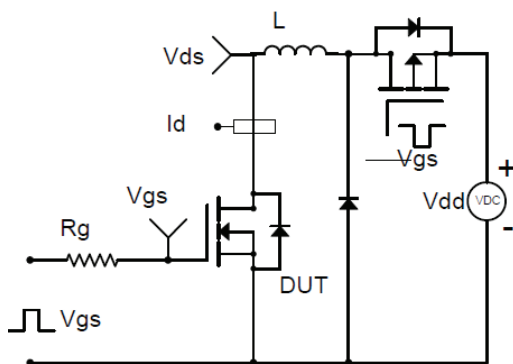
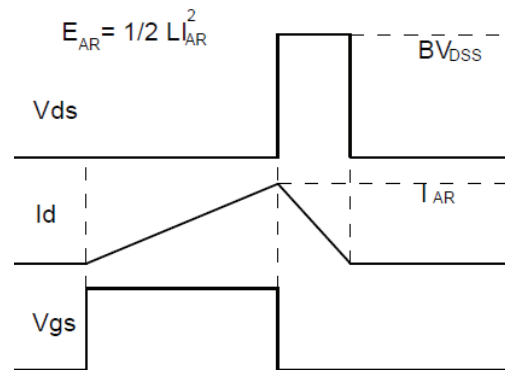
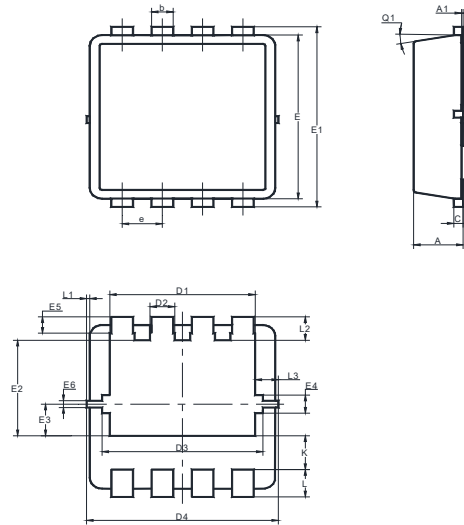


Fig.3-2 Avalanche waveform



Package Outline Dimensions (Units: mm)

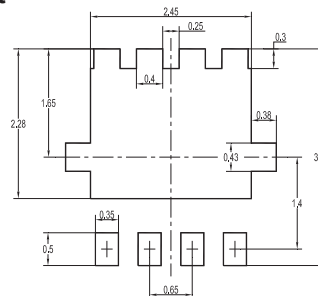
DFN3030



UNIT	A	A1	b	c	D1	D2	D3	D4	E	E1	E2	E3	E4
mm	0.9	0.05	0.35	0.25	2.6	0.5	2.7	3.2	3.1	3.3	1.85	0.68	0.43
	0.7	0	0.24	0.1	2.4	0.3	2.5	3	2.9	3.1	1.65	0.48	0.23

UNIT	E5	E6	e	K	L	L1	L2	L3	θ1
mm	0.4	0.25	0.7	0.72	0.5	0.1	0.53	0.475	12°
	0.2	0.15	0.6	0.52	0.3	0	0.33	0.275	0°

Recommended Soldering Footprint



Packing information

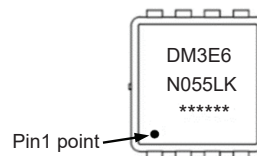
Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
DFN3030	12	8 ± 0.1	0.315 ± 0.004	330	13	5,000

Marking information

" DM3E6N055LK " = Part No.

" ***** " = Date Code Marking

Font type: Arial



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Fig. 7 Typical Junction Capacitance

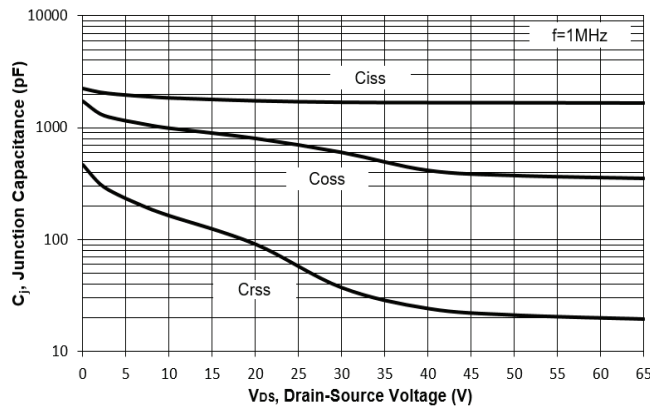


Fig. 8 Drain-Source Leakage Current vs. T_j

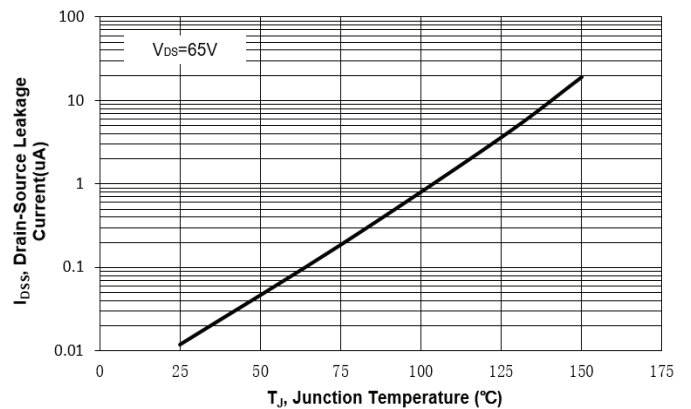


Fig. 9 V_{(BR)DSS} vs. Junction Temperature

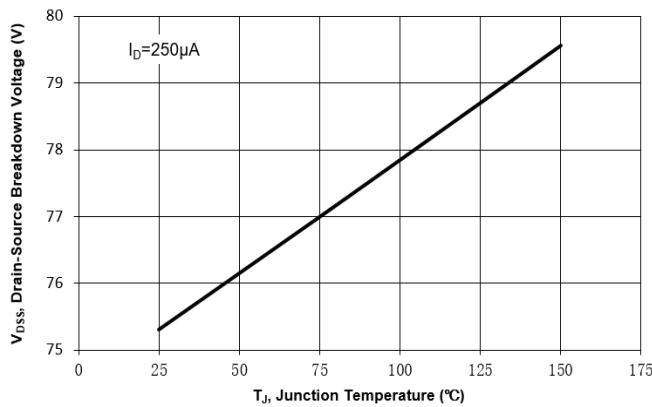


Fig. 10 Gate Threshold Variation vs. T_j

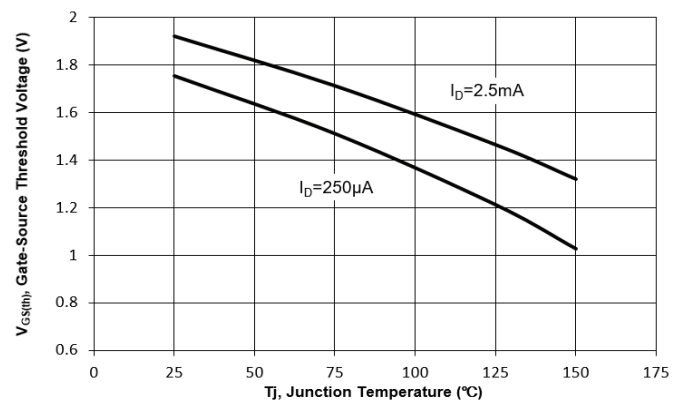


Fig. 11 Gate Charge

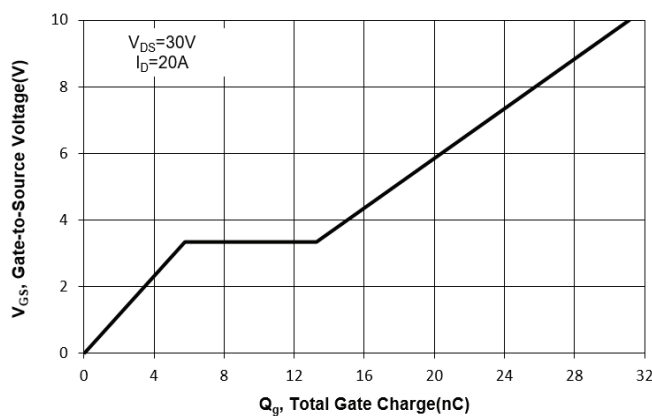


Fig. 12 Safe Operation Area

