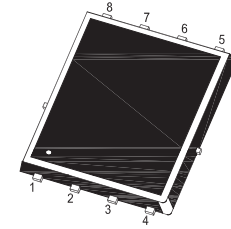
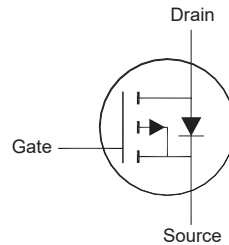


P-Channel Enhancement Mode MOSFET

Features

- Surface-mounted package
- Low Gate-Source Threshold Voltage
- Halogen and Antimony Free(HAF), RoHS compliant



1.Source 2.Source 3.Source 4.Gate
5.Drain 6.Drain 7.Drain 8.Drain
DFN5060 Plastic Package

Key Parameters

Parameter	Value	Unit
$-BV_{DS}$	40	V
$R_{DS(ON)}$ Max	19 @ $-V_{GS} = 10$ V	m Ω
	29 @ $-V_{GS} = 4.5$ V	
$-V_{GS(th)}$ typ	1.7	V
Q_g typ	42 @ $-V_{GS} = 10$ V	nC

Absolute Maximum Ratings (at $T_a = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DS}$	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	$-I_D$	32	A
$T_c = 25^\circ\text{C}$ $T_c = 100^\circ\text{C}$		20	
Peak Drain Current ¹⁾	$-I_{DM}$	130	A
Avalanche Current	$-I_{AS}$	29	A
Avalanche Energy ²⁾	E_{AS}	42	mJ
Power Dissipation	P_D	31.2	W
$T_c = 25^\circ\text{C}$			
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	4	$^\circ\text{C/W}$
Thermal Resistance from Junction to Ambient ³⁾	$R_{\theta JA}$	50	$^\circ\text{C/W}$

¹⁾ Pulse Test: Pulse Width ≤ 100 μs , Duty Cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.

²⁾ Limited by $T_{J(MAX)}$, starting $T_J = 25^\circ\text{C}$, $L = 0.1$ mH, $R_g = 25$ Ω , $I_{AS} = 29$ A, $V_{GS} = 10$ V.

³⁾ Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

Characteristics at T_a = 25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at $-I_D = 250 \mu A$	$-V_{(BR)DSS}$	40	-	-	V
Drain-Source On-State Current at $-V_{DS} = 40 V$	$-I_{DSS}$	-	-	1	μA
Gate-Source Leakage Current at $V_{GS} = \pm 20 V$	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at $V_{DS} = V_{GS}$, $-I_D = 250 \mu A$	$-V_{GS(th)}$	1	-	2.5	V
Drain-Source On-State Resistance at $-V_{GS} = 10 V$, $-I_D = 10 A$ at $-V_{GS} = 4.5 V$, $-I_D = 8 A$	$R_{DS(on)}$	- -	15 -	19 29	m Ω
DYNAMIC PARAMETERS					
Forward Transconductance at $-V_{DS} = 5 V$, $-I_D = 10 A$	g_{fs}	-	25	-	S
Gate resistance at $V_{GS} = 0 V$, $V_{DS} = 0 V$, $f = 1 MHz$	R_g	-	5.1	-	Ω
Input Capacitance at $V_{GS} = 0 V$, $-V_{DS} = 20 V$, $f = 1 MHz$	C_{iss}	-	2573	-	pF
Output Capacitance at $V_{GS} = 0 V$, $-V_{DS} = 20 V$, $f = 1 MHz$	C_{oss}	-	174	-	pF
Reverse Transfer Capacitance at $V_{GS} = 0 V$, $-V_{DS} = 20 V$, $f = 1 MHz$	C_{rss}	-	111	-	pF
Total Gate Charge at $-V_{GS} = 10 V$, $-V_{DS} = 20 V$, $-I_D = 10 A$ at $-V_{GS} = 4.5 V$, $-V_{DS} = 20 V$, $-I_D = 10 A$	Q_g	- -	42 19	- -	nC
Gate-Source Charge at $-V_{GS} = 10 V$, $-V_{DS} = 20 V$, $-I_D = 10 A$	Q_{gs}	-	8.5	-	nC
Gate-Drain Charge at $-V_{GS} = 10 V$, $-V_{DS} = 20 V$, $-I_D = 10 A$	Q_{gd}	-	5.5	-	nC
Turn-On Delay Time at $-V_{GS} = 10 V$, $-V_{DS} = 20 V$, $-I_D = 10 A$, $R_g = 3.3 \Omega$	$t_{d(on)}$	-	14	-	ns
Turn-On Rise Time at $-V_{GS} = 10 V$, $-V_{DS} = 20 V$, $-I_D = 10 A$, $R_g = 3.3 \Omega$	t_r	-	26	-	ns
Turn-Off Delay Time at $-V_{GS} = 10 V$, $-V_{DS} = 20 V$, $-I_D = 10 A$, $R_g = 3.3 \Omega$	$t_{d(off)}$	-	27	-	ns
Turn-Off Fall Time at $-V_{GS} = 10 V$, $-V_{DS} = 20 V$, $-I_D = 10 A$, $R_g = 3.3 \Omega$	t_f	-	5	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at $-I_S = 1 A$, $-V_{GS} = 0 V$	$-V_{SD}$	-	-	1.2	V
Body-Diode Continuous Current	$-I_S$	-	-	32	A
Body-Diode Continuous Current, Pulsed	$-I_{SM}$	-	-	130	A
Body Diode Reverse Recovery Time at $-I_S = 10 A$, $di/dt = 100 A / \mu s$	t_{rr}	-	14.5	-	ns
Body Diode Reverse Recovery Charge at $-I_S = 10 A$, $di/dt = 100 A / \mu s$	Q_{rr}	-	9.3	-	nC

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

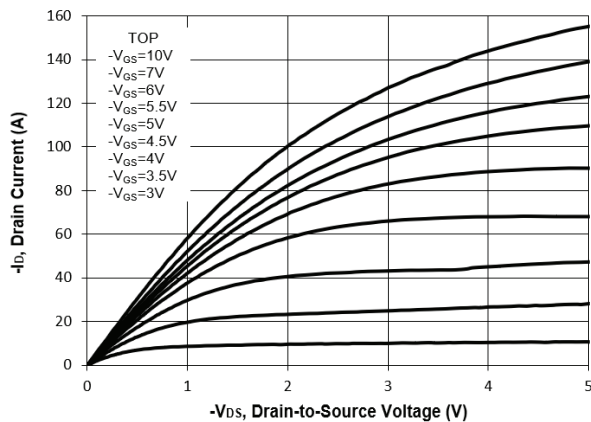


Fig. 2 Typical Transfer Characteristics

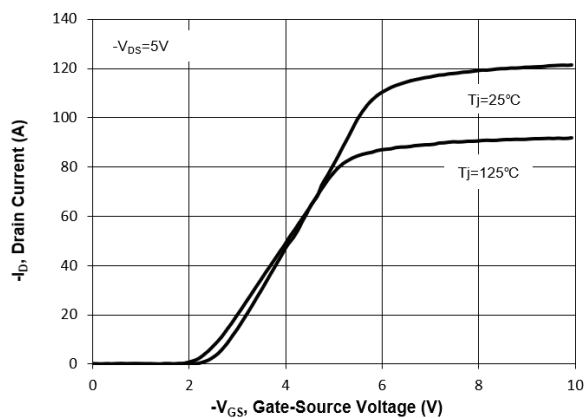


Fig. 3 on-Resistance vs. Drain Current

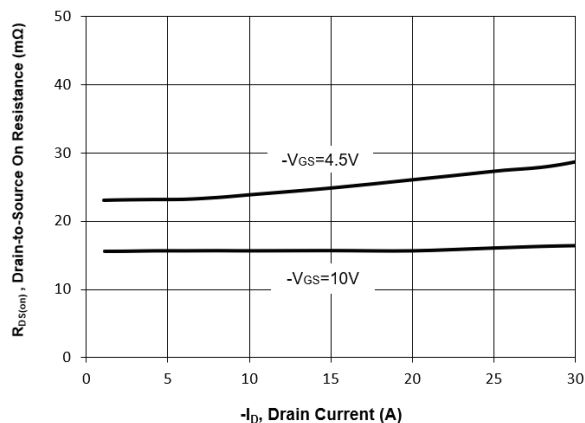


Fig. 4 on-Resistance vs. Gate to Source Voltage

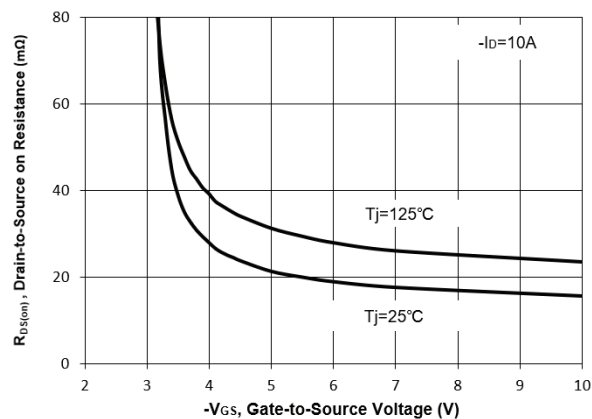


Fig. 5 on-Resistance vs. TJ

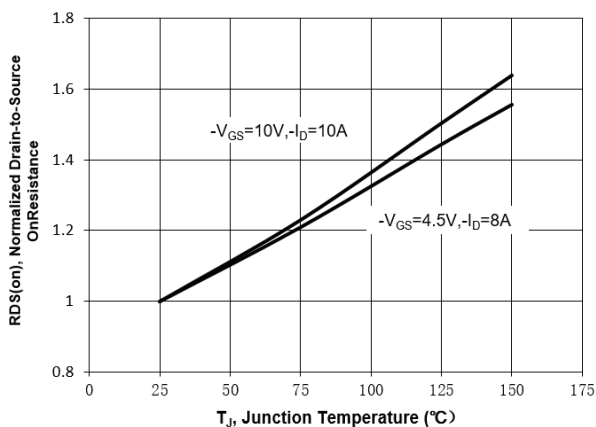
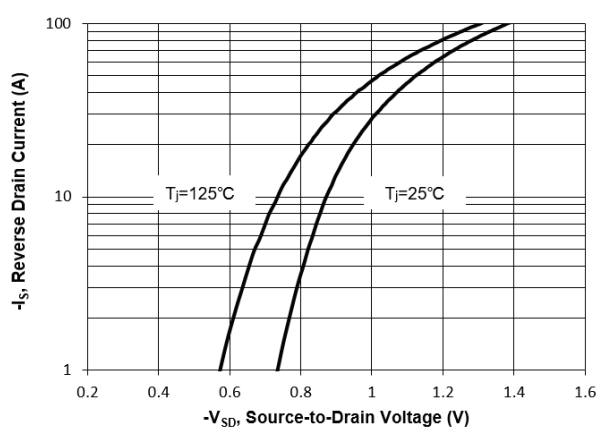


Fig. 6 Typical Body-Diode Forward Characteristics



Electrical Characteristics Curves

Fig. 7 Typical Junction Capacitance

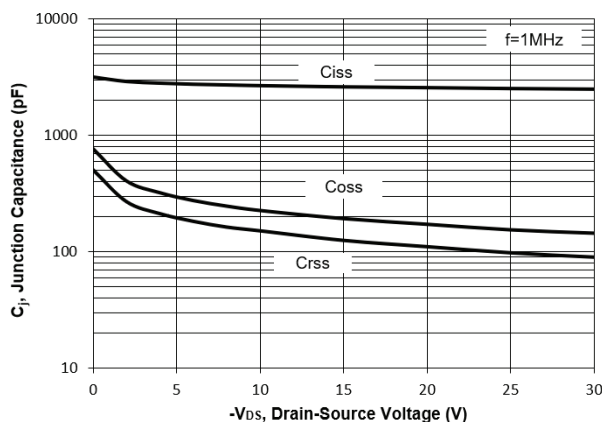


Fig. 8 Drain-Source Leakage Current vs. T_j

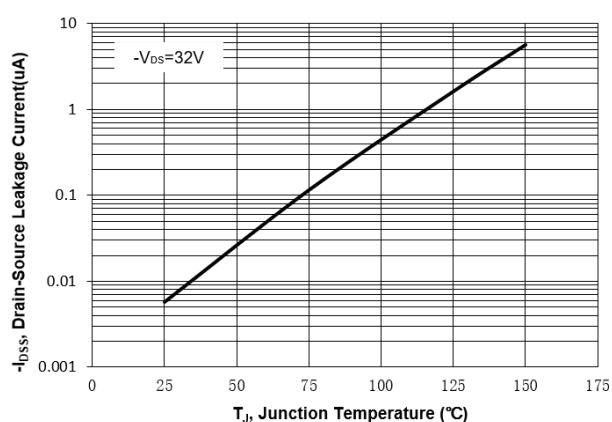


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

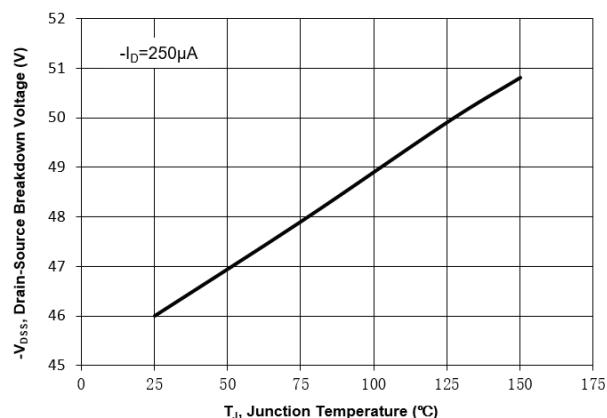


Fig. 10 Gate Threshold Variation vs. T_j

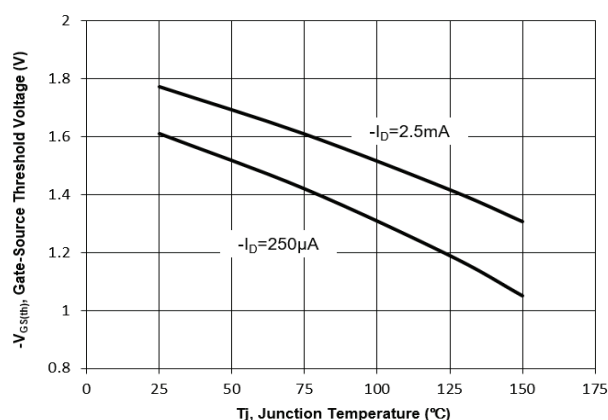


Fig. 11 Gate Charge

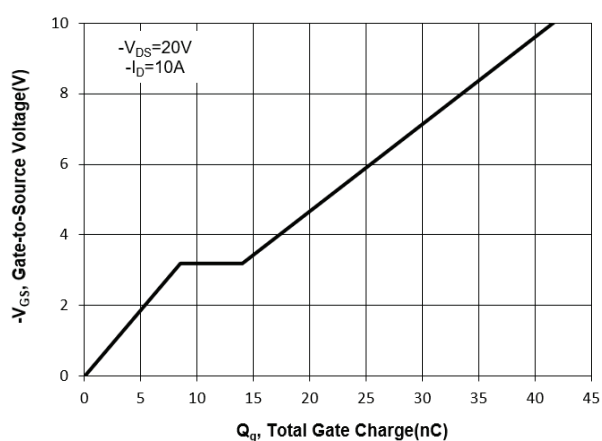


Fig. 12 Safe Operation Area

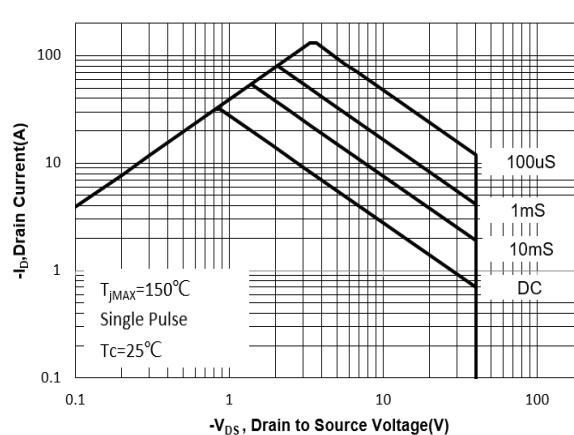


Fig.13 Normalized Maximum Transient Thermal Impedance($Z_{\theta JC}$)

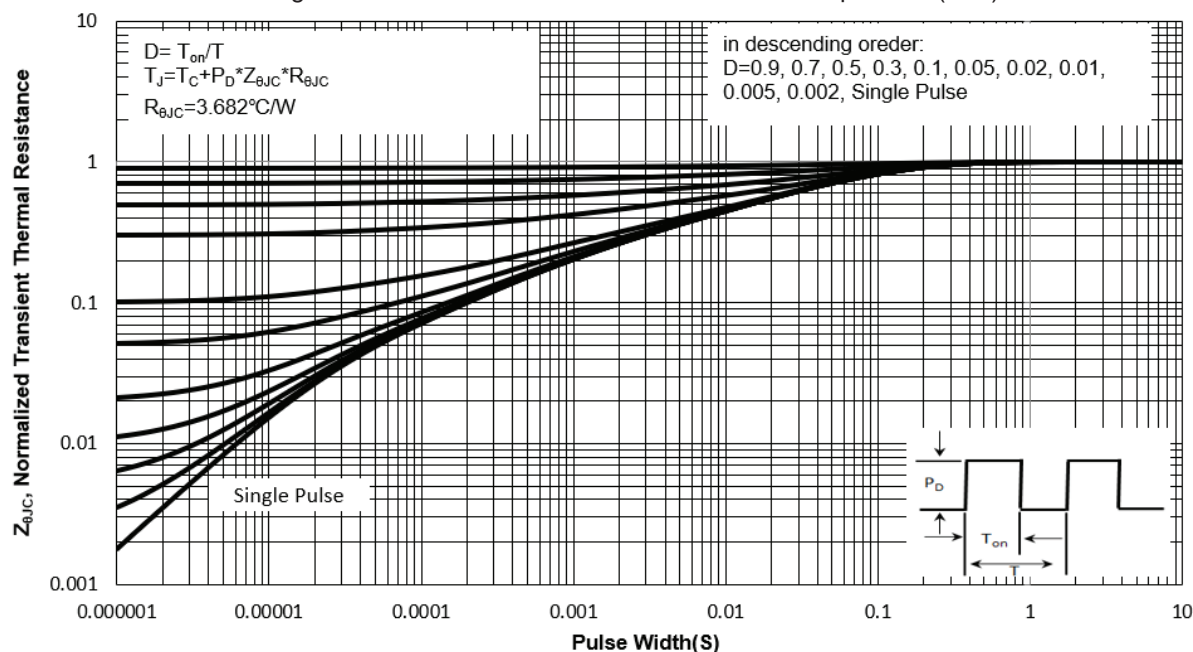
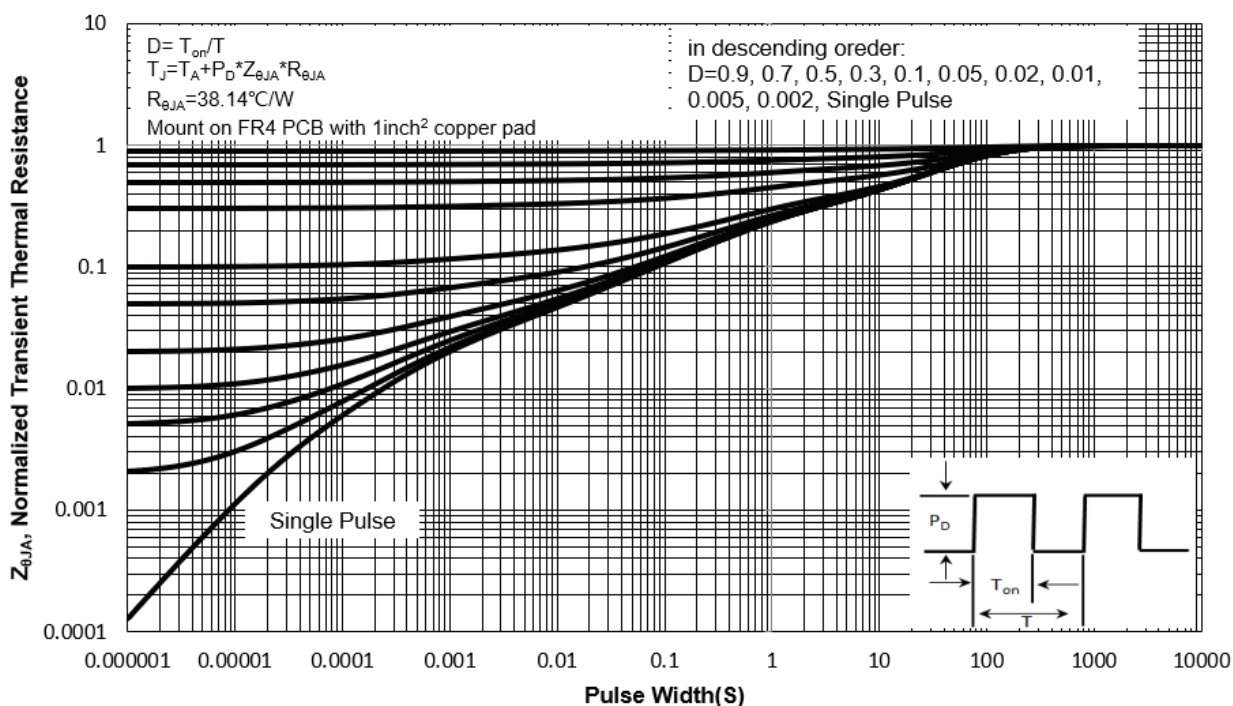


Fig.14 Normalized Maximum Transient Thermal Impedance($Z_{\theta JA}$)



Test Circuits

Fig.1-1 Switching times test circuit

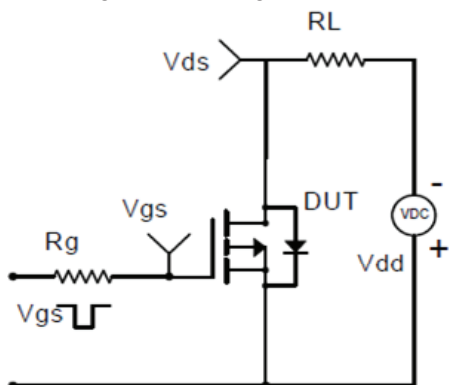


Fig.1-2 Switching Waveform

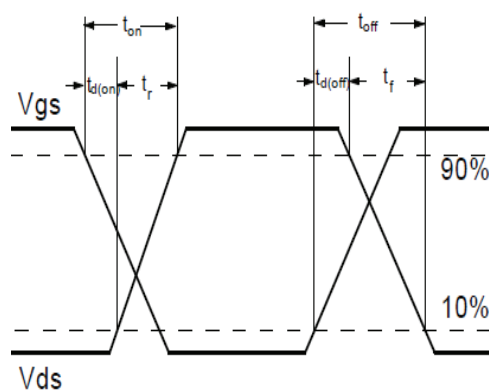


Fig.2-1 Gate charge test circuit

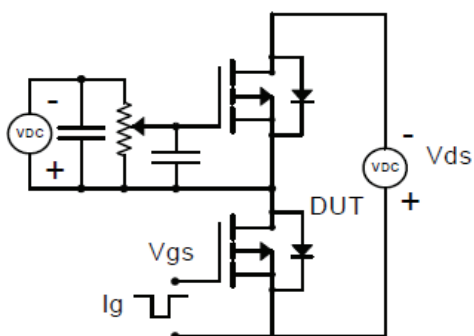


Fig.2-2 Gate charge waveform

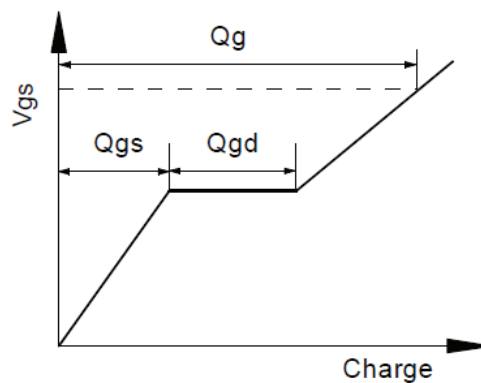


Fig.3-1 Avalanche test circuit

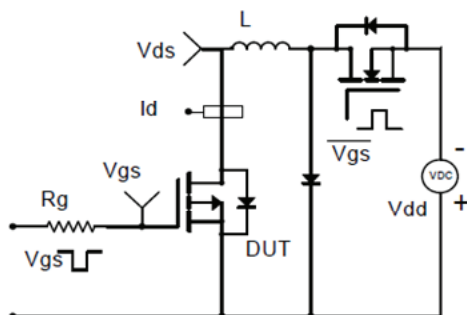
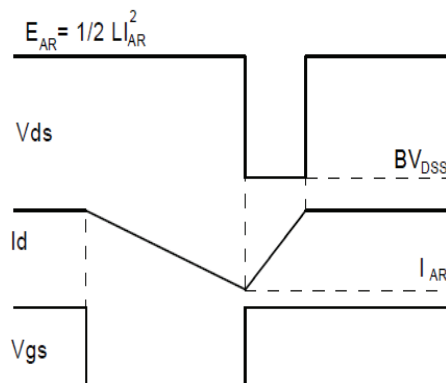
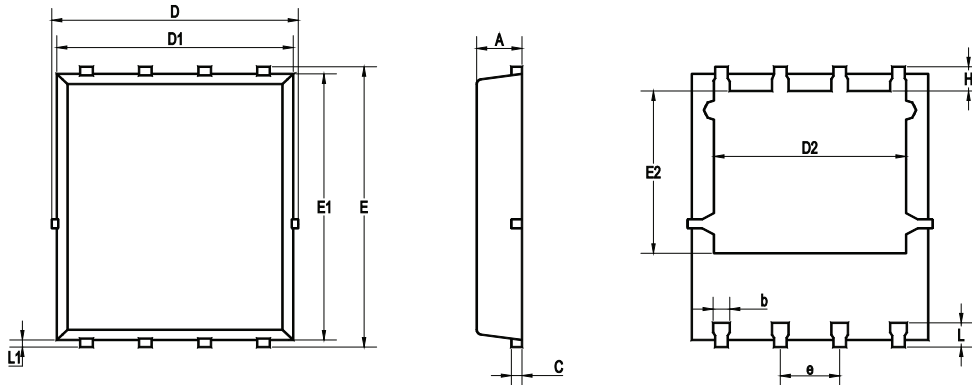


Fig.3-2 Avalanche waveform



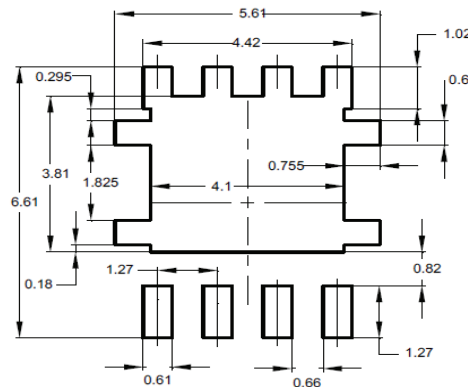
Package Outline Dimensions (Units: mm)

DFN5060



UNIT	A	b	C	D	D1	D2	E	E1	E2	e	L	L1	H
mm	1.12 0.9	0.51 0.33	0.34 0.11	5.26 4.7	5.1 4.7	4.5 3.56	6.25 5.75	6 5.6	3.66 3.18	1.37 1.17	0.71 0.35	0.2 0.06	0.71 0.35

Recommended Soldering Footprint



Packing information

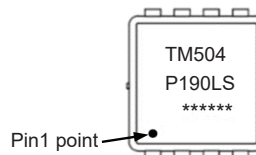
Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
DFN5060	12	8 ± 0.1	0.315 ± 0.004	330	13	5,000

Marking information

" TM504P190LS " = Part No.

" ***** " = Date Code Marking

Font type: Arial



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