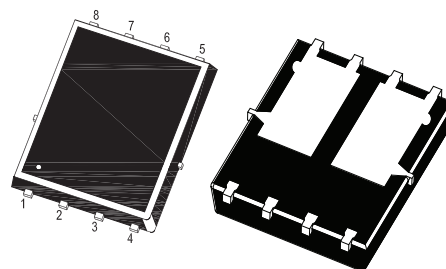
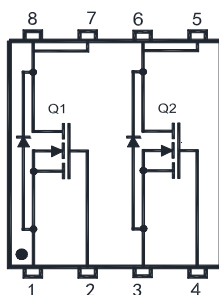


Dual N-Channel Enhancement Mode MOSFET

Features

- Low $R_{DS(ON)}$
- Surface-mounted package
- Low Gate-Source Threshold Voltage
- Halogen and Antimony Free(HAF), RoHS compliant



Q1:1.Source 2.Gate 7.Drain 8.Drain
 Q2:3.Source 4.Gate 5.Drain 6.Drain
 DFN5060 Plastic Package

Key Parameters(Q1/Q2)

Parameter	Value	Unit
BV_{DSS}	60	V
$R_{DS(ON)} \text{ Max}$	8.5 @ $V_{GS} = 10 \text{ V}$	m Ω
	10.5 @ $V_{GS} = 4.5 \text{ V}$	
$V_{GS(th)} \text{ typ}$	1.6	V
$Q_g \text{ typ}$	36.4 @ $V_{GS} = 10 \text{ V}$	nC

Absolute Maximum Ratings (at $T_a = 25^\circ\text{C}$ unless otherwise specified) (Q1/Q2)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	I_D	54	A
		37	
Peak Drain Current, Pulsed ¹⁾	I_{DM}	280	A
Avalanche Current	I_{AS}	36	A
Single Pulse Avalanche Energy ²⁾	E_{AS}	65	mJ
Total Power Dissipation	P_{tot}	40.5	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	$^\circ\text{C}$

Thermal Characteristics(Q1/Q2)

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	3.7	$^\circ\text{C/W}$
Thermal Resistance from Junction to Ambient ³⁾	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$

¹⁾ Pulse Test: Pulse Width $\leq 100 \mu\text{s}$, Duty Cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 175^\circ\text{C}$.

²⁾ Limited by $T_{J(MAX)}$, starting $T_J = 25^\circ\text{C}$, $L = 0.1 \text{ mH}$, $R_g = 25 \Omega$, $I_{AS} = 36 \text{ A}$, $V_{GS} = 10 \text{ V}$.

³⁾ Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

Characteristics at $T_a = 25^\circ\text{C}$ unless otherwise specified(Q1/Q2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at $I_D = 1\text{ mA}$	BV_{DSS}	60	-	-	V
Drain-Source Leakage Current at $V_{DS} = 48\text{ V}$	I_{DSS}	-	-	1	μA
Gate Leakage Current at $V_{GS} = \pm 16\text{ V}$	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	$V_{GS(th)}$	1.2	-	2.5	V
Drain-Source On-State Resistance at $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$ at $V_{GS} = 4.5\text{ V}$, $I_D = 15\text{ A}$	$R_{DS(on)}$	- -	6.8 -	8.5 10.5	$\text{m}\Omega$
DYNAMIC PARAMETERS					
Forward Transconductance at $V_{DS} = 5\text{ V}$, $I_D = 15\text{ A}$	g_{fs}	-	29	-	S
Gate resistance at $V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V}$, $f = 1\text{ MHz}$	R_g	-	1	-	Ω
Input Capacitance at $V_{GS} = 0\text{ V}$, $V_{DS} = 30\text{ V}$, $f = 1\text{ MHz}$	C_{iss}	-	1609	-	pF
Output Capacitance at $V_{GS} = 0\text{ V}$, $V_{DS} = 30\text{ V}$, $f = 1\text{ MHz}$	C_{oss}	-	616	-	pF
Reverse Transfer Capacitance at $V_{GS} = 0\text{ V}$, $V_{DS} = 30\text{ V}$, $f = 1\text{ MHz}$	C_{rss}	-	32	-	pF
Gate charge total at $V_{DS} = 30\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$ at $V_{DS} = 30\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 4.5\text{ V}$	Q_g	- -	36.4 19.3	- -	nC
Gate to Source Charge at $V_{DS} = 30\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$	Q_{gs}	-	5.8	-	nC
Gate to Drain Charge at $V_{DS} = 30\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$	Q_{gd}	-	10.5	-	nC
Turn-On Delay Time at $V_{DS} = 30\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 3.3\text{ }\Omega$	$t_{d(on)}$	-	14	-	ns
Turn-On Rise Time at $V_{DS} = 30\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 3.3\text{ }\Omega$	t_r	-	29	-	ns
Turn-Off Delay Time at $V_{DS} = 30\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 3.3\text{ }\Omega$	$t_{d(off)}$	-	14	-	ns
Turn-Off Fall Time at $V_{DS} = 30\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$, $R_g = 3.3\text{ }\Omega$	t_f	-	3	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at $I_S = 1\text{ A}$, $V_{GS} = 0\text{ V}$	V_{SD}	-	-	1.3	V
Body-Diode Continuous Current	I_S	-	-	54	A
Body-Diode Continuous Current, Pulsed	I_{SM}	-	-	280	A
Body Diode Reverse Recovery Time at $I_S = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	t_{rr}	-	38	-	ns
Body Diode Reverse Recovery Charge at $I_S = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	Q_{rr}	-	38	-	nC

Electrical Characteristics Curves (Q1/Q2)

Fig. 1 Typical Output Characteristics

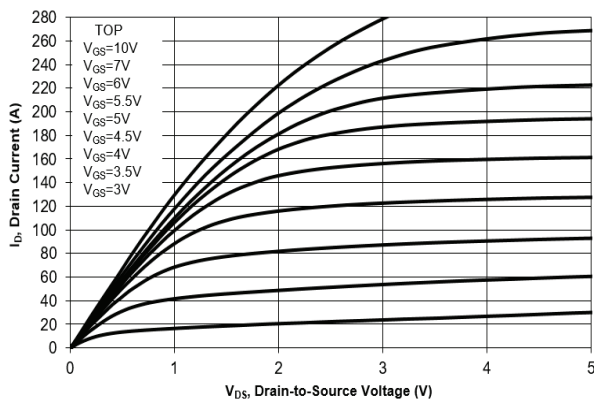


Fig. 2 Typical Transfer Characteristics

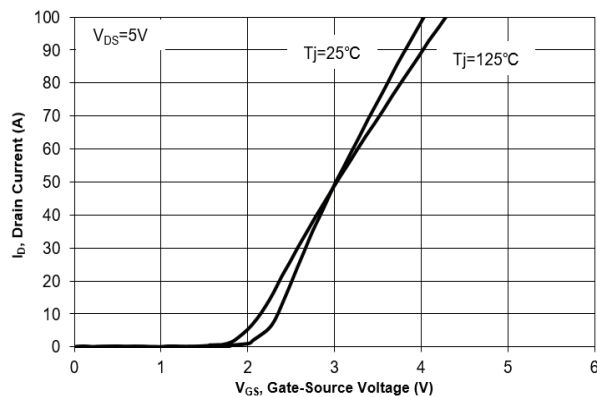


Fig. 3 on-Resistance vs. Drain Current

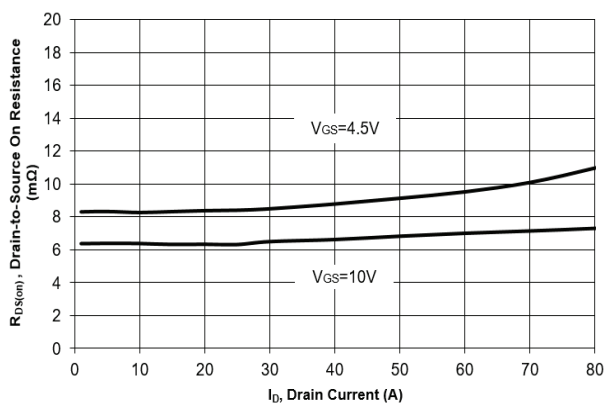


Fig. 4 on-Resistance vs. Gate to Source Voltage

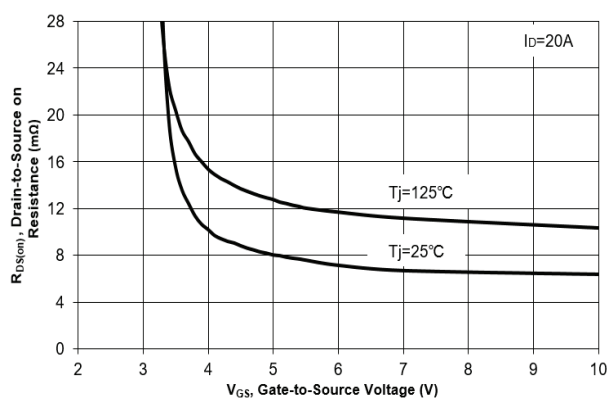


Fig. 5 on-Resistance vs. T_J

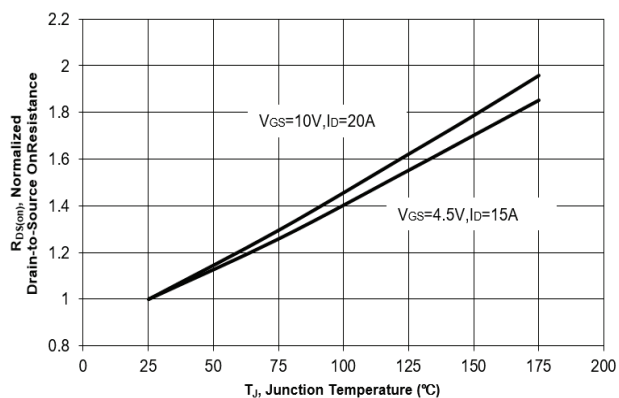
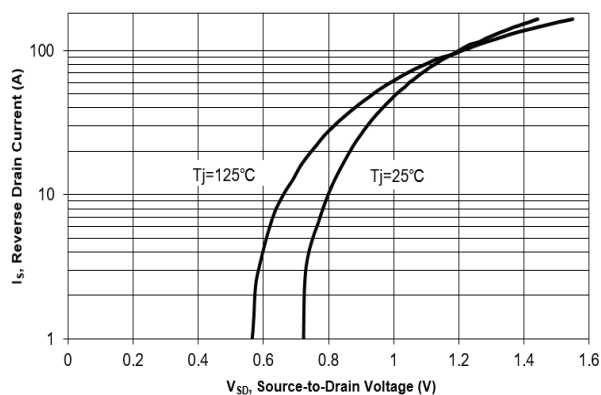


Fig. 6 Typical Body-Diode Forward Characteristics



Electrical Characteristics Curves(Q1/Q2)

Fig. 13 Normalized Maximum Transient Thermal Impedance($Z_{\theta JC}$)

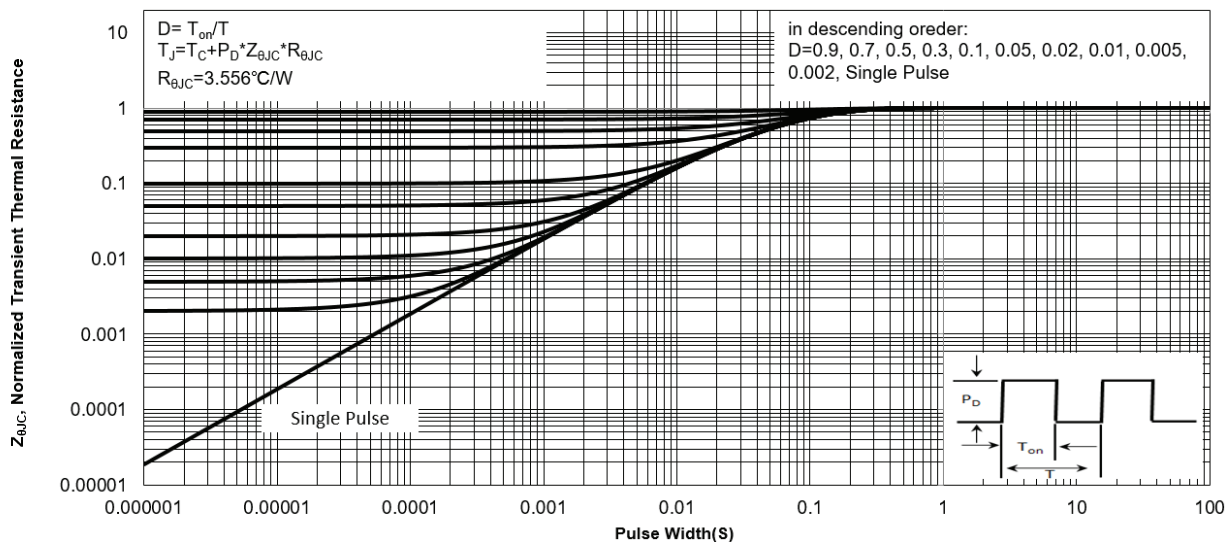


Fig. 14 Normalized Maximum Transient Thermal Impedance($Z_{\theta JA}$)

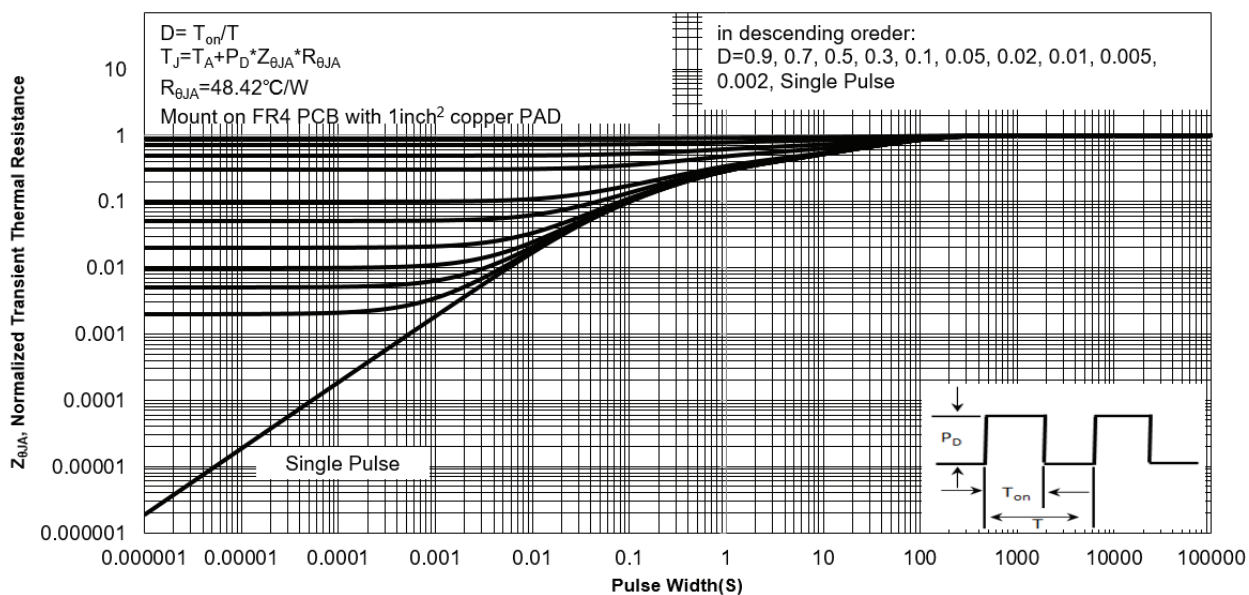


Fig. 7 Typical Junction Capacitance

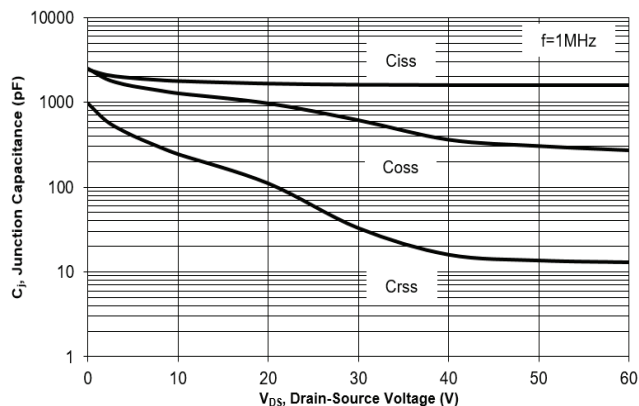


Fig. 8 Drain-Source Leakage Current vs. T_J

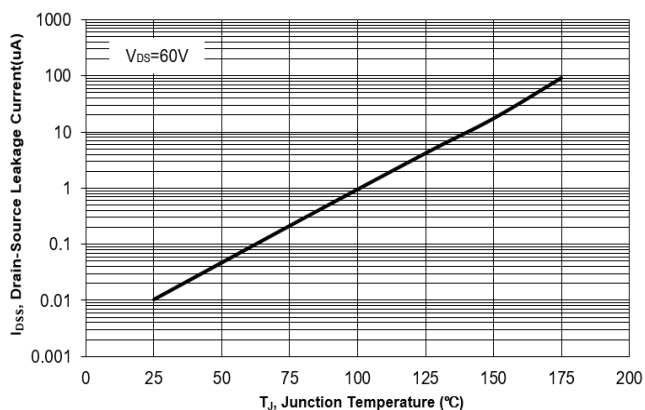


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

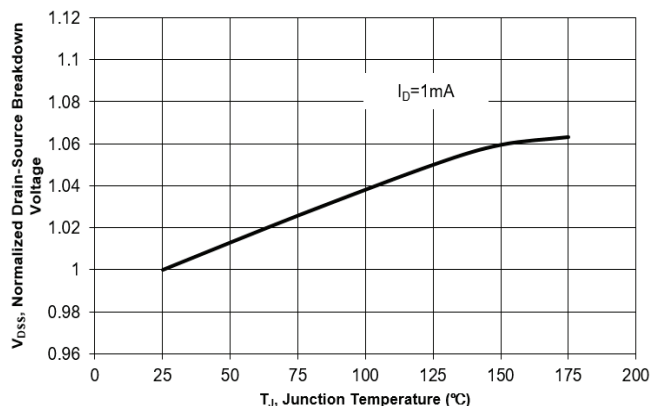


Fig. 10 Gate Threshold Variation vs. T_J

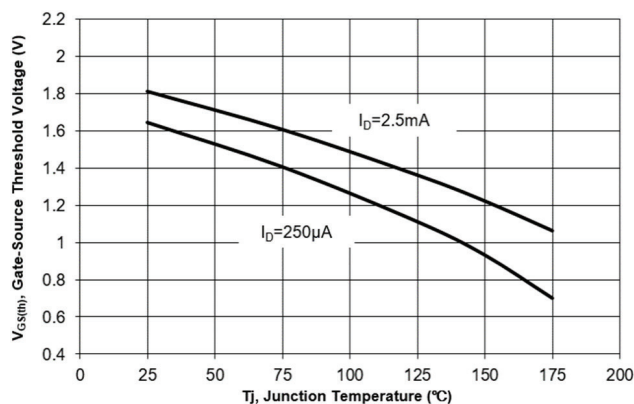


Fig. 11 Gate Charge

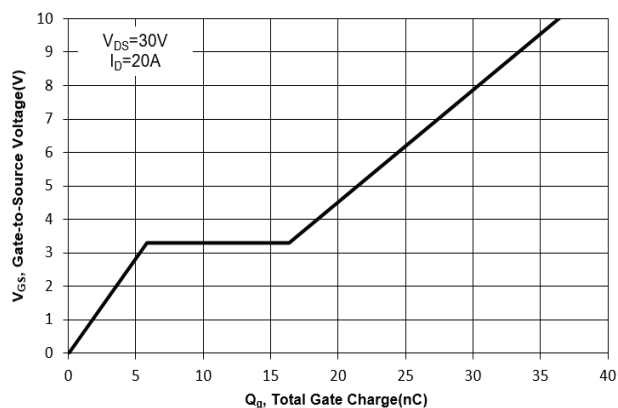
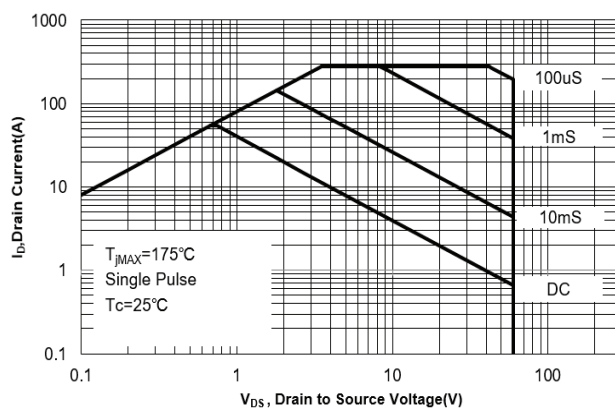
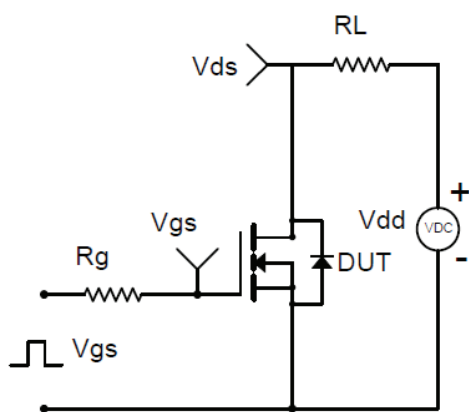
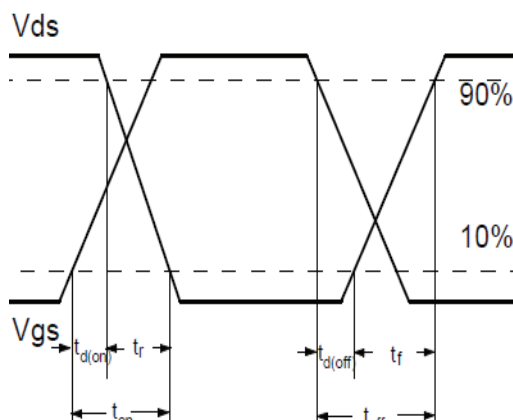
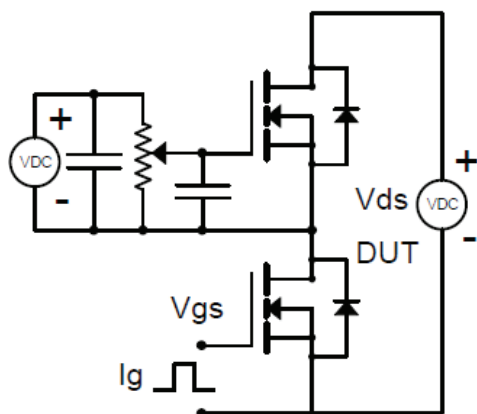
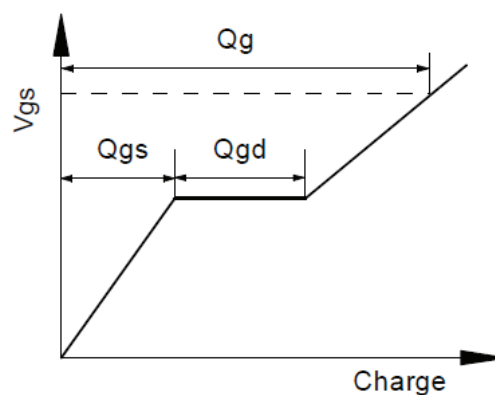
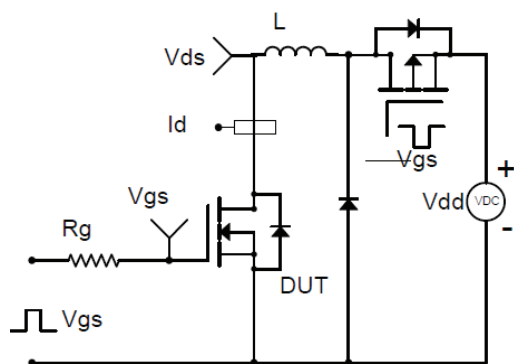
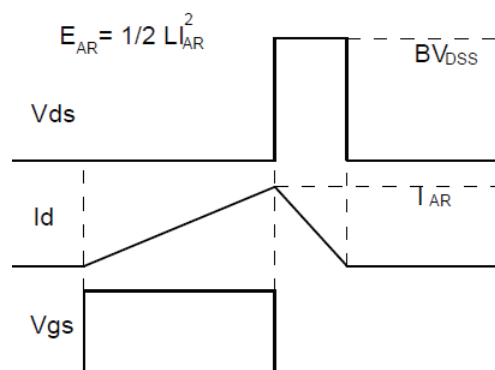


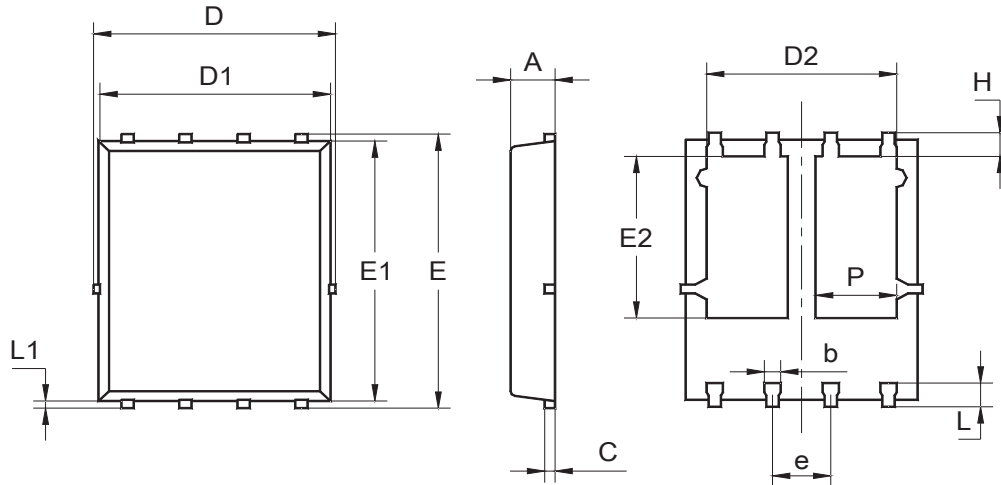
Fig. 12 Safe Operation Area



Test Circuits(Q1/Q2)
Fig.1-1 Switching times test circuit

Fig.1-2 Switching Waveform

Fig.2-1 Gate charge test circuit

Fig.2-2 Gate charge waveform

Fig.3-1 Avalanche test circuit

Fig.3-2 Avalanche waveform


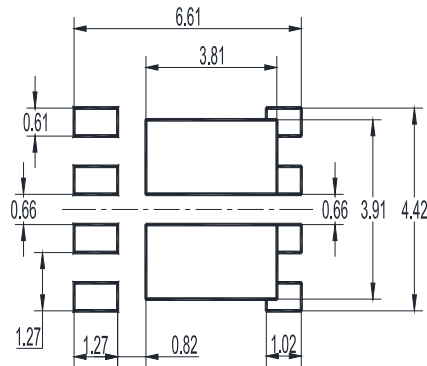
Package Outline Dimensions (Units: mm)

DFN5060



Unit	A	b	C	D	D1	D2	E	E1	E2	e	L	L1	H	P
mm	1.12 0.9	0.51 0.33	0.34 0.11	5.26 4.7	5.1 4.7	4.5 3.56	6.25 5.75	6 5.6	3.66 3.18	1.37 1.17	0.71 0.35	0.2 0.06	0.71 0.35	2.0 1.6

Recommended Soldering Footprint



Packing information

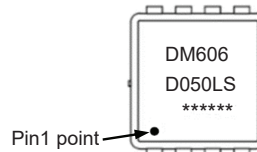
Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
DFN5060	12	8 ± 0.1	0.315 ± 0.004	330	13	5,000

Marking information

" DM606D050LS " = Part No

" ***** " = Date Code Marking

Font type: Arial



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