

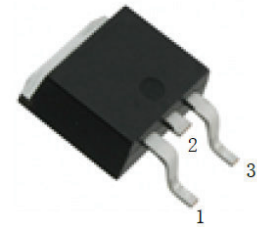
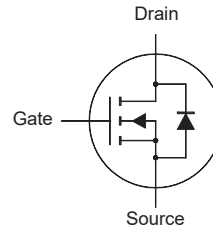
N-Channel Enhancement Mode MOSFET

Features

- Low gate charge
- Fast switching speed
- Halogen and Antimony Free(HAF),
RoHS compliant

Applications

- Power management for UPS and inverter systems



1.Gate 2.Drain 3.Source
TO-252 Plastic Package

Key Parameters

Parameter	Value	Unit
BV_{DSS}	40	V
$R_{DS(ON)} \text{ Max}$	6 @ $V_{GS} = 10 \text{ V}$	m Ω
$V_{GS(th)} \text{ typ}$	2.5	V
$Q_g \text{ typ}$	110 @ $V_{GS} = 10 \text{ V}$	nC

Absolute Maximum Ratings (at $T_a = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	I_D	90 57	A
Peak Drain Current, Pulsed ¹⁾	I_{DM}	480	A
Avalanche Current	I_{AS}	25	A
Single-Pulse Avalanche Energy ²⁾	E_{AS}	312	mJ
Power Dissipation	P_D	75	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2	$^\circ\text{C/W}$
Thermal Resistance from Junction to Ambient ³⁾	$R_{\theta JA}$	40	$^\circ\text{C/W}$

¹⁾ Pulse Test: Pulse Width $\leq 100 \mu\text{s}$, Duty Cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 175^\circ\text{C}$.

²⁾ Limited by $T_{J(MAX)}$, starting $T_J = 25^\circ\text{C}$, $L = 1 \text{ mH}$, $R_g = 25 \Omega$, $I_D = 25 \text{ A}$, $V_{GS} = 10 \text{ V}$.

³⁾ Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

Characteristics at T_a = 25°C unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I _D = 250 μA	BV _{DSS}	40	-	-	V
Drain-Source Leakage Current at V _{DS} = 40 V	I _{DSS}	-	-	1	μA
Gate Leakage Current at V _{GS} = ± 20 V	I _{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at V _{DS} = V _{GS} , I _D = 250 μA	V _{GS(th)}	2	-	4	V
Drain-Source On-State Resistance at V _{GS} = 10 V, I _D = 40 A	R _{DS(on)}	-	4.6	6	mΩ
DYNAMIC PARAMETERS					
Gate Resistance at V _{DS} = 0 V, f = 1 MHz	R _g	-	1	-	Ω
Input Capacitance at V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz	C _{iss}	-	5660	-	pF
Output Capacitance at V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz	C _{oss}	-	624	-	pF
Reverse Transfer Capacitance at V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz	C _{rss}	-	398	-	pF
Gate charge total at V _{DD} = 20 V, V _{GS} = 10 V, I _D = 40 A	Q _g	-	110	-	nC
Gate to Source Charge at V _{DD} = 20 V, V _{GS} = 10 V, I _D = 40 A	Q _{gs}	-	25	-	nC
Gate to Drain Charge at V _{DD} = 20 V, V _{GS} = 10 V, I _D = 40 A	Q _{gd}	-	29	-	nC
Turn-On Delay Time at V _{DD} = 20 V, V _{GS} = 10 V, I _D = 40 A, R _g = 4.7 Ω	t _{d(on)}	-	45	-	ns
Turn-On Rise Time at V _{DD} = 20 V, V _{GS} = 10 V, I _D = 40 A, R _g = 4.7 Ω	t _r	-	84	-	ns
Turn-Off Delay Time at V _{DD} = 20 V, V _{GS} = 10 V, I _D = 40 A, R _g = 4.7 Ω	t _{d(off)}	-	34	-	ns
Turn-Off Fall Time at V _{DD} = 20 V, V _{GS} = 10 V, I _D = 40 A, R _g = 4.7 Ω	t _f	-	13	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I _S = 1 A, V _{GS} = 0 V	V _{SD}	-	-	1.3	V
Body-Diode Continuous Current	I _S	-	-	90	A
Body-Diode Continuous Current, Pulsed	I _{SM}	-	-	480	A
Body Diode Reverse Recovery Time at I _S = 40 A, di/dt = 100 A / μs	t _{rr}	-	23	-	ns
Body Diode Reverse Recovery Charge at I _S = 40 A, di/dt = 100 A / μs	Q _{rr}	-	17	-	nC

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

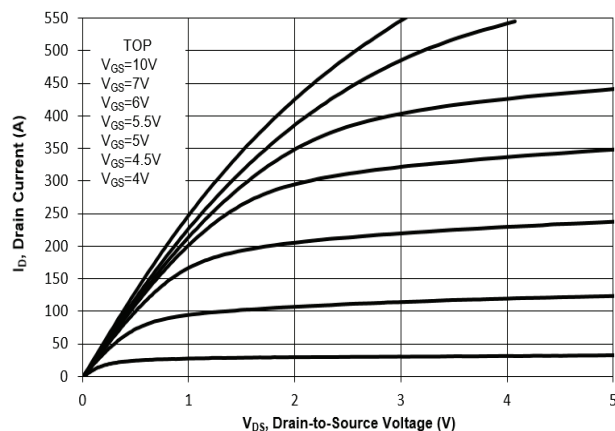


Fig. 2 Typical Transfer Characteristics

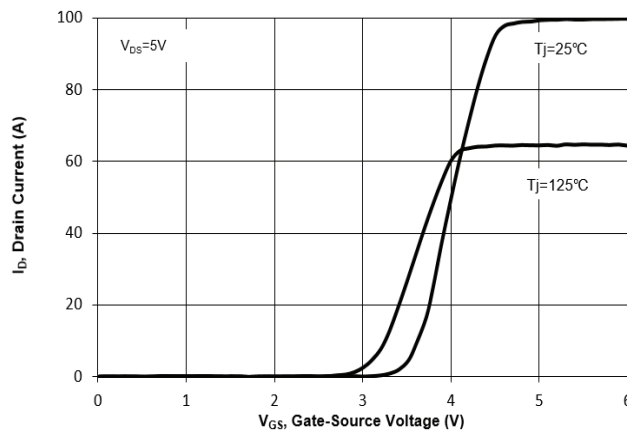


Fig. 3 on-Resistance vs. Drain Current

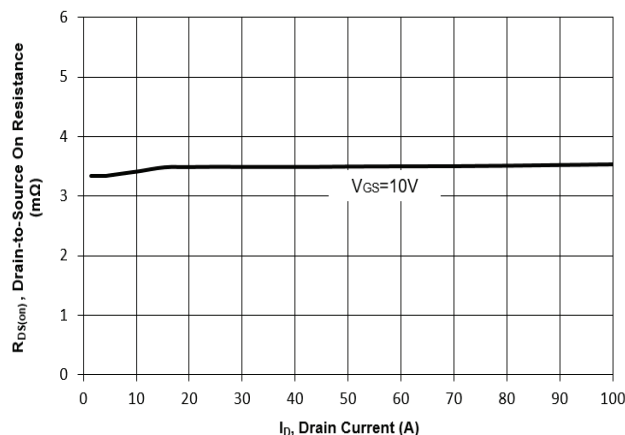


Fig. 4 on-Resistance vs. Gate to Source Voltage

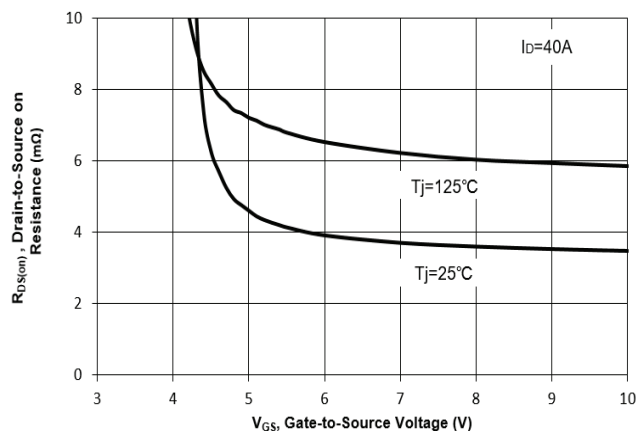


Fig. 5 on-Resistance vs. T_J

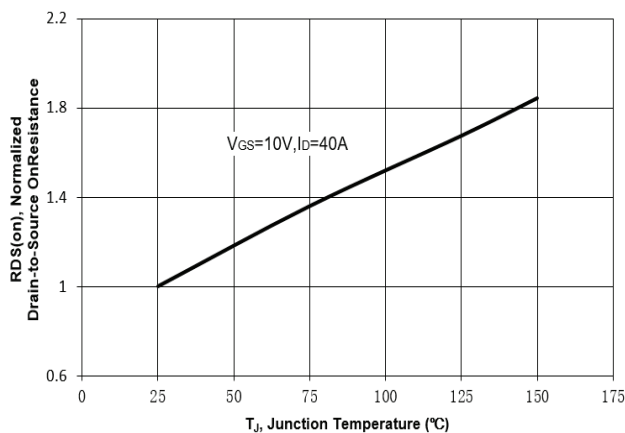
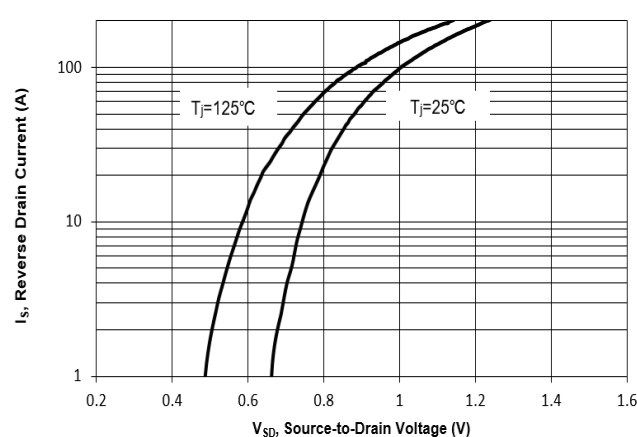


Fig. 6 Typical Body-Diode Forward Characteristics



Electrical Characteristics Curves

Fig. 13 Normalized Maximum Transient Thermal Impedance($z_{\theta JC}$)

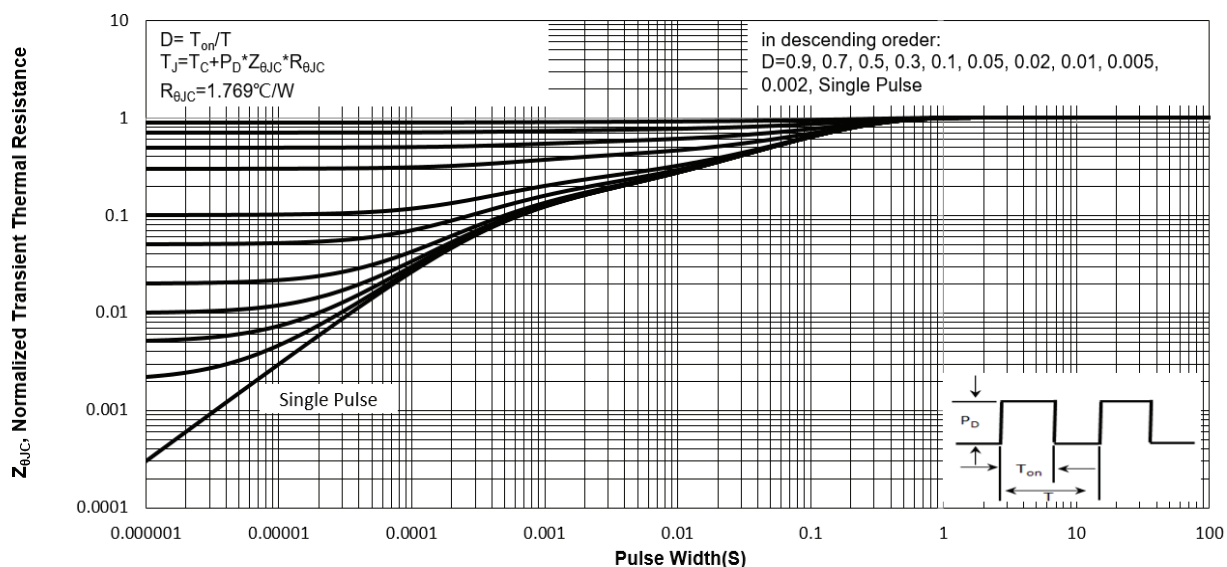
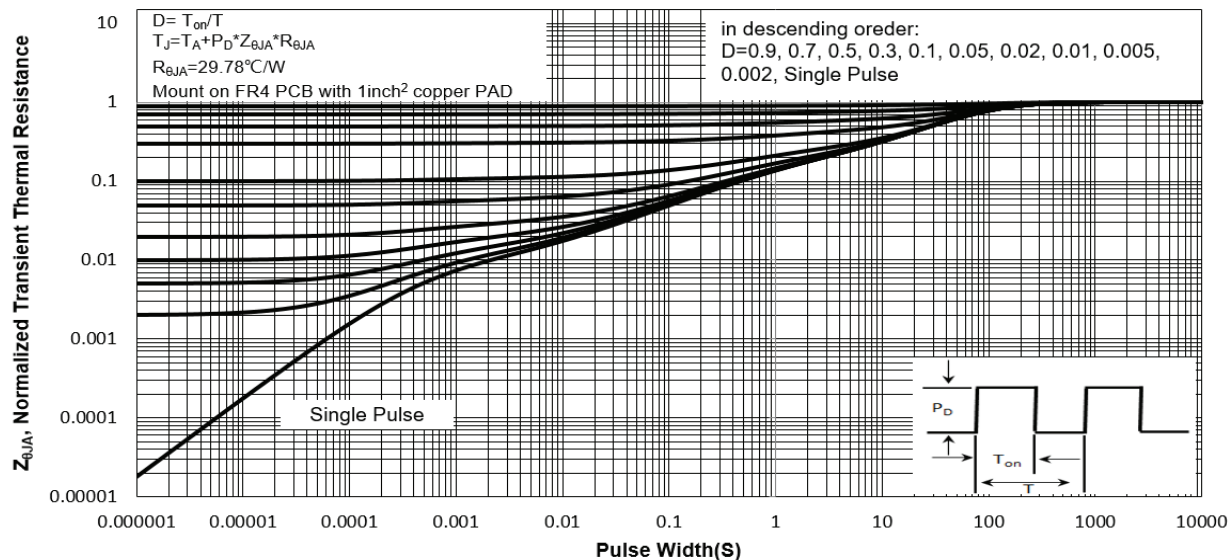


Fig. 14 Normalized Maximum Transient Thermal Impedance($z_{\theta JA}$)



Test Circuits

Fig.1-1 Switching times test circuit

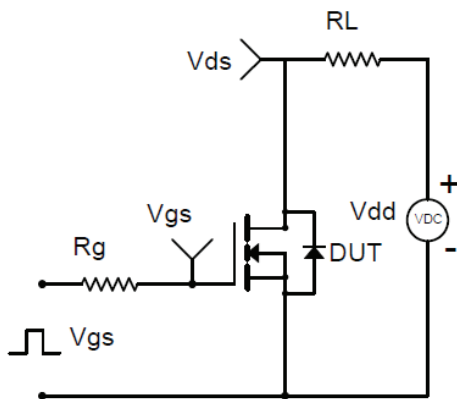


Fig.1-2 Switching Waveform

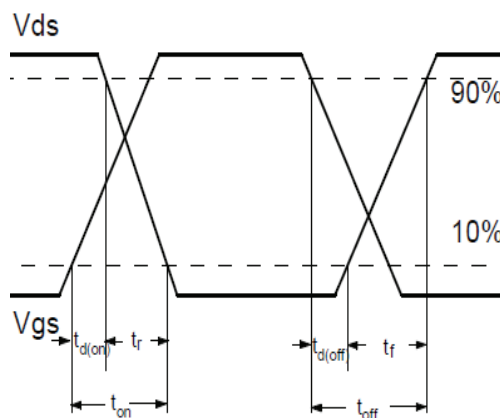


Fig.2-1 Gate charge test circuit

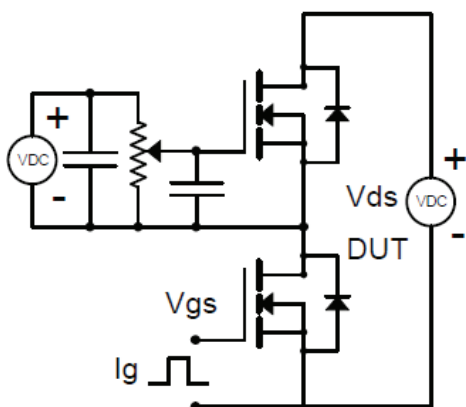


Fig.2-2 Gate charge waveform

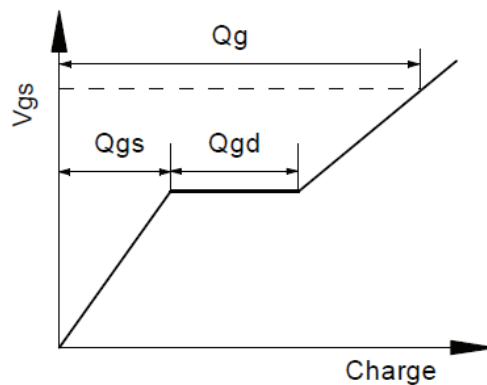


Fig.3-1 Avalanche test circuit

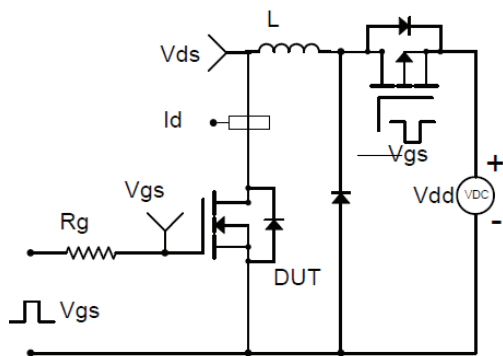
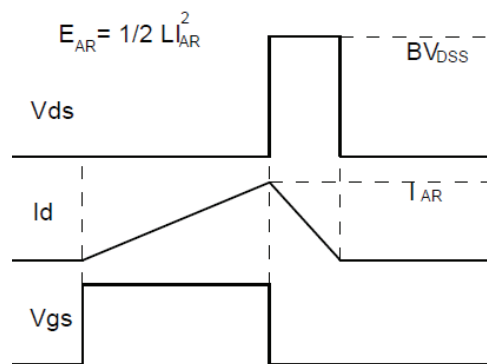
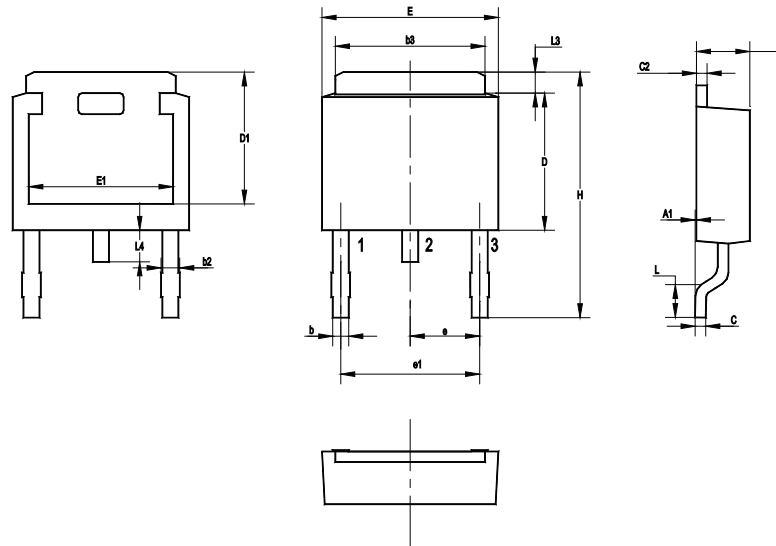


Fig.3-2 Avalanche waveform



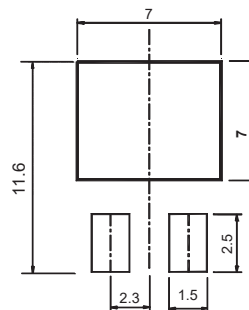
Package Outline Dimensions (Units: mm)

TO-252



UNIT	A	A1	b	b2	b3	C	C2	D	D1	E	E1	e	e1	H	L	L3	L4
mm	2.5	0.15	1.0	1.15	5.5	0.65	0.65	6.2	5.4	6.7	5.0	2.30	4.60	10.7	1.78	1.20	1.10
	2.1	0	0.5	0.65	4.9	0.4	0.4	5.6	5.0	6.1	4.6	TYP.	TYP.	9	1.40	0.85	0.51

Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
TO-252	16	8 ± 0.1	0.315 ± 0.004	330	13	2,500

Marking information

" SFTN8046R " = Part No.

" ***** " = Date Code Marking

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Electrical Characteristics Curves

Fig. 7 Typical Junction Capacitance

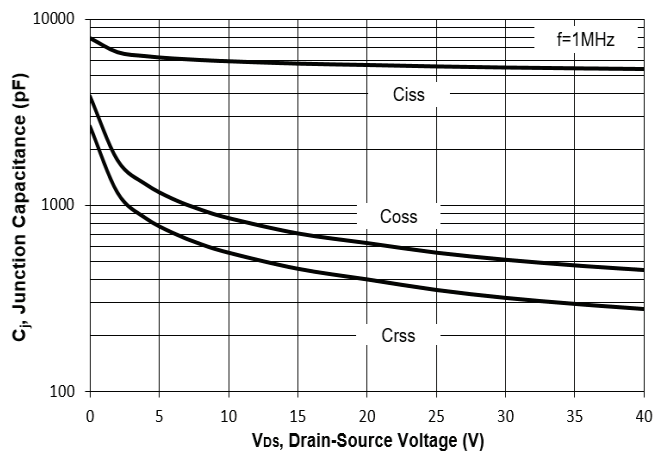


Fig. 8 Drain-Source Leakage Current vs. T_J

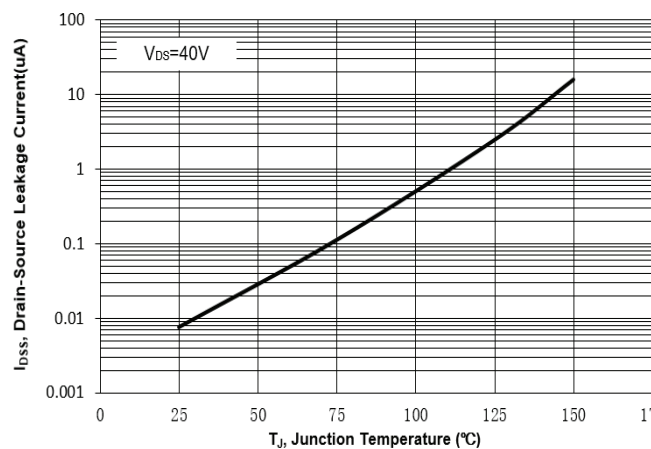


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

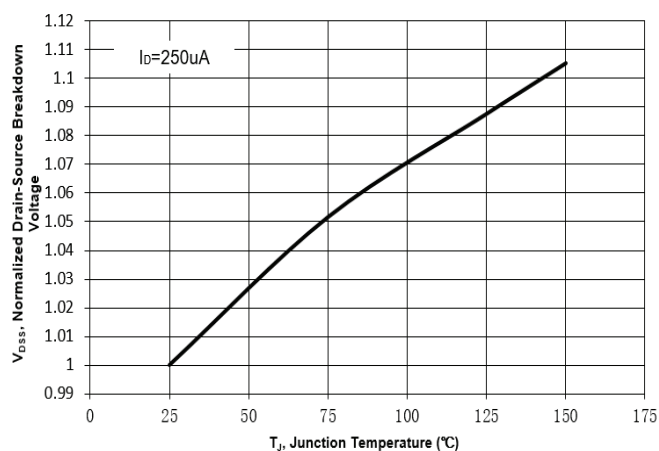


Fig. 10 Gate Threshold Variation vs. T_J

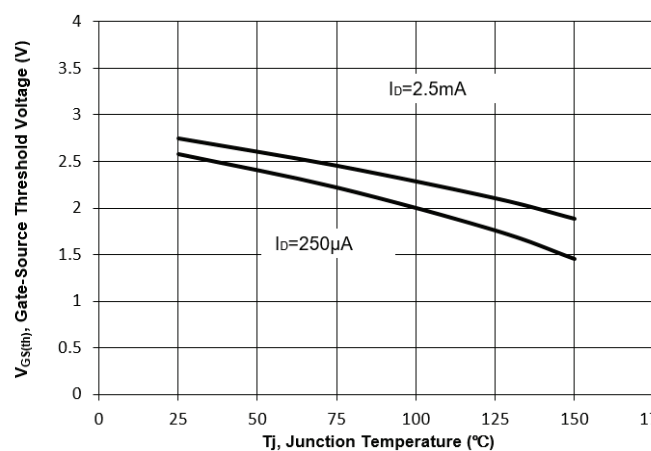


Fig. 11 Gate Charge

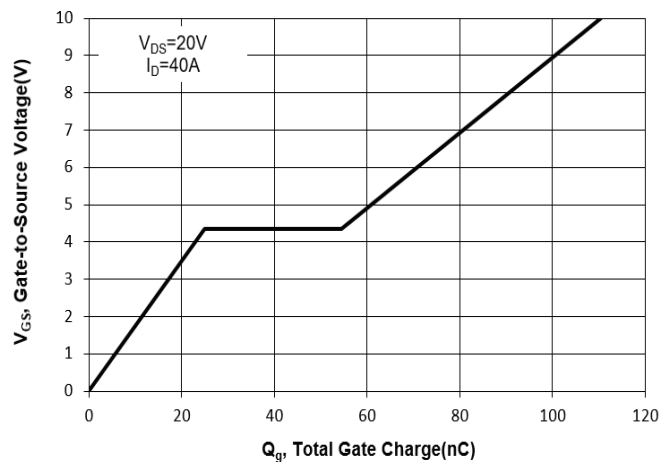


Fig. 12 Safe Operation Area

