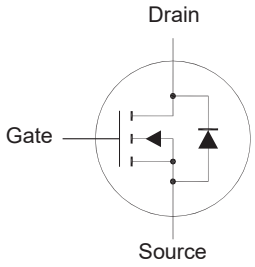
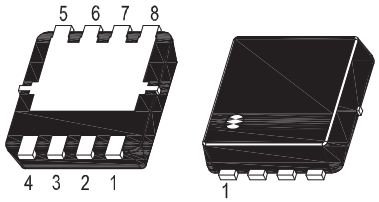
N-Channel Enhancement Mode MOSFET

Features

- Surface-mounted package
- Low Gate-Source Threshold Voltage
- Halogen and Antimony Free(HAF) RoHS compliant





1. Source 2. Source 3. Source 4. Gate
5. Drain 6. Drain 7. Drain 8. Drain
DFN3030 Plastic Package

Key Parameters

Parameter	Value	Unit
BV_{DSS}	40	V
$R_{DS(ON)}$ Max	5.7 @ V_{GS} = 10 V	mΩ
	7 @ V_{GS} = 4.5 V	
$V_{GS(th)}$ typ	1.6	V
Q_g typ	69.9 @ V_{GS} = 10 V	nC

Absolute Maximum Ratings (at T_a = 25℃ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current - Continuous	T_c = 25℃	I_D	52	A
	T_c = 100℃		32	
Drain Current Pulsed [1]		I_{DM}	220	A
Avalanche Current		I_{AS}	20.3	A
Single Pulse Avalanche Energy [2]		E_{AS}	103	mJ
Power Dissipation	T_c = 25℃	P_D	30	W
Operating Junction and Storage Temperature Range		T_j, T_{stg}	- 55 to + 175	℃

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	5	℃/W
Thermal Resistance from Junction to Ambient [3]	$R_{\theta JA}$	58	℃/W

[1] Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ = 175°C.
[2] Limited by $T_{J(MAX)}$, starting T_J = 25 °C, L = 0.5 mH, R_g = 25 Ω, I_{AS} = 20.3 A, V_{GS} = 10 V.
[3] Device Surface Mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate, in a still air.

Surge Components Inc. (USA)
sales@surgecomponents.com
+1 (631) 595-1818

Surge Components EMEA (Europe)
roger@surgecomponents.com
+44-203-983-9133

Surge Components.Ltd. (Asia)
surgehk@surgecomponents.com.hk
+852-2172-7607

Characteristics at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I_D = 250 µA	BV_{DSS}	40	-	-	V
Drain-Source Leakage Current at V_{DS} = 32 V	I_{DSS}	-	-	1	µA
Gate-Source Leakage Current at V_{GS} = ± 20 V	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 µA	$V_{GS(th)}$	1	-	2.5	V
Drain-Source On-State Resistance at V_{GS} = 10 V, I_D = 10 A at V_{GS} = 4.5 V, I_D = 5 A	$R_{DS(on)}$	- -	4.6 -	5.7 7	mΩ
DYNAMIC PARAMETERS					
Forward Transconductance at V_{DS} = 5 V, I_D = 5 A	g_{fs}	-	18.8	-	S
Gate resistance at V_{GS} = 0 V, V_{DS} = 0 V, f = 1 MHz	R_g	-	0.5	-	Ω
Input Capacitance at V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz	C_{iss}	-	3255	-	pF
Output Capacitance at V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz	C_{oss}	-	260	-	pF
Reverse Transfer Capacitance at V_{GS} = 0 V, V_{DS} = 20 V, f = 1 MHz	C_{rss}	-	195	-	pF
Gate charge total at V_{DS} = 20 V, I_D = 10 A, V_{GS} = 10 V at V_{DS} = 20 V, I_D = 10 A, V_{GS} = 4.5 V	Q_g	- -	69.9 33	- -	nC
Gate to Source Charge at V_{DS} = 20 V, I_D = 10 A, V_{GS} = 10 V	Q_{gs}	-	10	-	nC
Gate to Drain Charge at V_{DS} = 20 V, I_D = 10 A, V_{GS} = 10 V	Q_{gd}	-	13	-	nC
Turn-On Delay Time at V_{DS} = 20 V, I_D = 10 A, V_{GS} = 10 V, R_g = 3.3 Ω	$t_{d(on)}$	-	22	-	ns
Turn-On Rise Time at V_{DS} = 20 V, I_D = 10 A, V_{GS} = 10 V, R_g = 3.3 Ω	t_r	-	26	-	ns
Turn-Off Delay Time at V_{DS} = 20 V, I_D = 10 A, V_{GS} = 10 V, R_g = 3.3 Ω	$t_{d(off)}$	-	21	-	ns
Turn-Off Fall Time at V_{DS} = 20 V, I_D = 10 A, V_{GS} = 10 V, R_g = 3.3 Ω	t_f	-	3	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I_S = 1 A, V_{GS} = 0 V	V_{SD}	-	-	1.2	V
Body-Diode Continuous Current	I_S	-	-	52	A
Body-Diode Continuous Current, Pulsed	I_{SM}	-	-	220	A
Body Diode Reverse Recovery Time at I_S = 10 A, di/dt = 100 A / µs	t_{rr}	-	16	-	ns
Body Diode Reverse Recovery Charge at I_S = 10 A, di/dt = 100 A / µs	Q_{rr}	-	9	-	nC

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Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

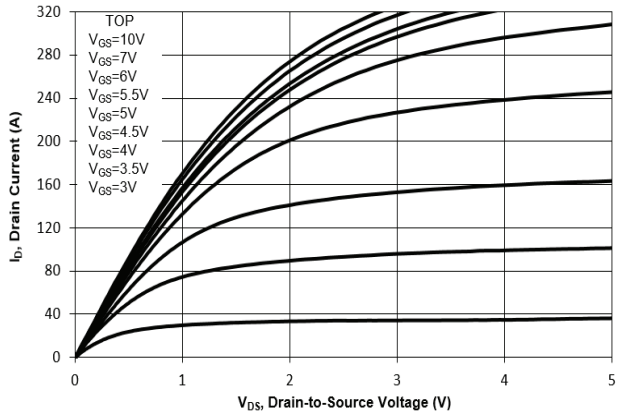


Fig. 2 Typical Transfer Characteristics

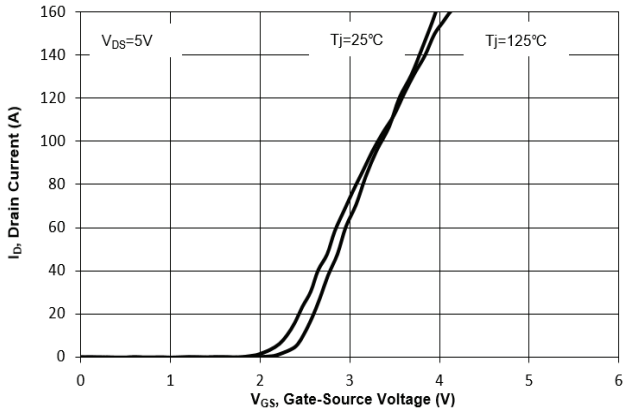


Fig. 3 On-Resistance vs. Drain Current

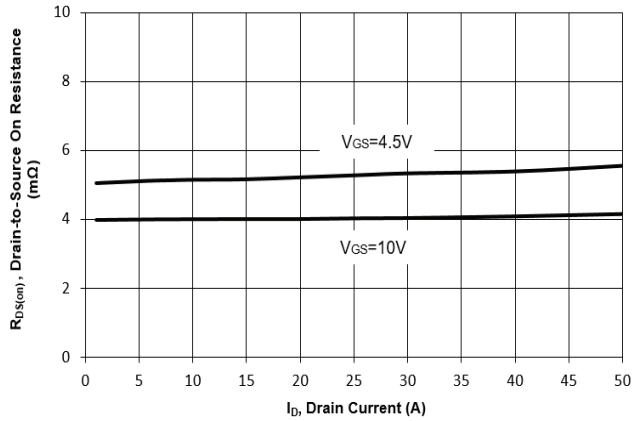


Fig. 4 On-Resistance vs. Gate to Source Voltage

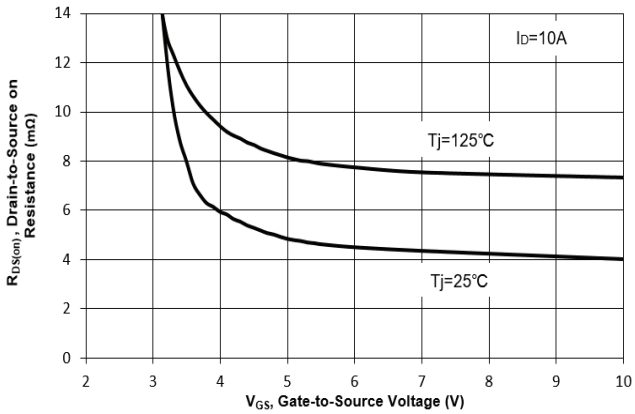


Fig. 5 On-Resistance vs.T_j

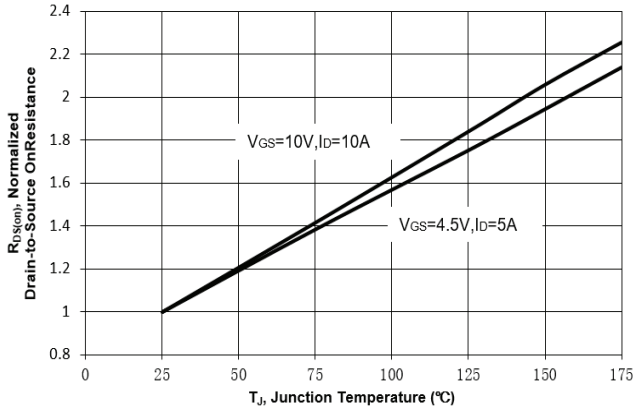
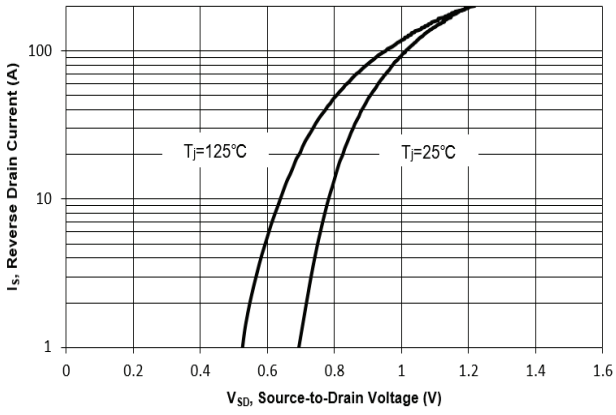


Fig. 6 Typical Body-Diode Forward Characteristics



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+852-2172-7607

Electrical Characteristics Curves

Fig. 7 Typical Junction Capacitance

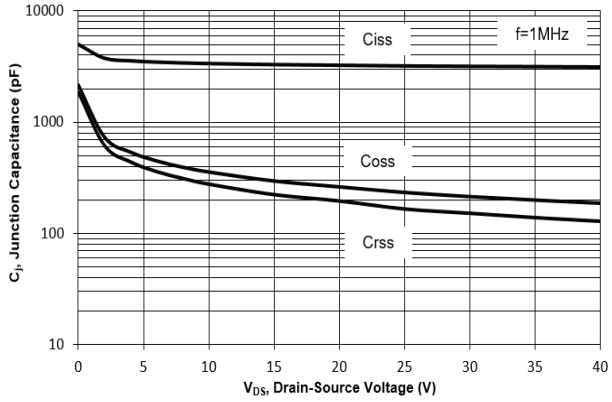


Fig. 8 Drain-Source Leakage Current vs. T_j

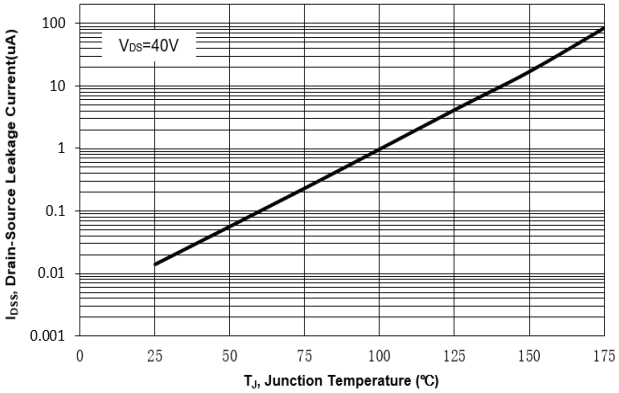


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

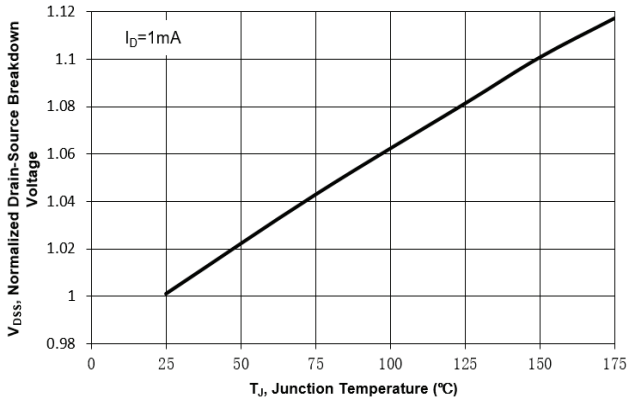


Fig. 10 Gate Threshold Variation vs. T_j

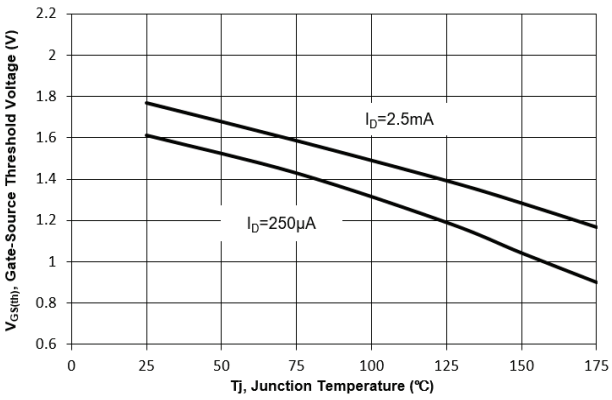


Fig. 11 Gate Charge

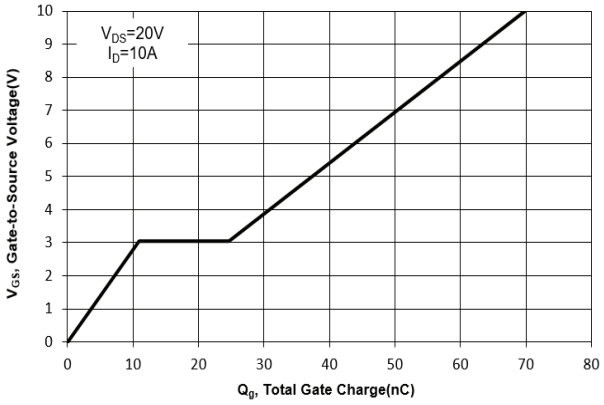
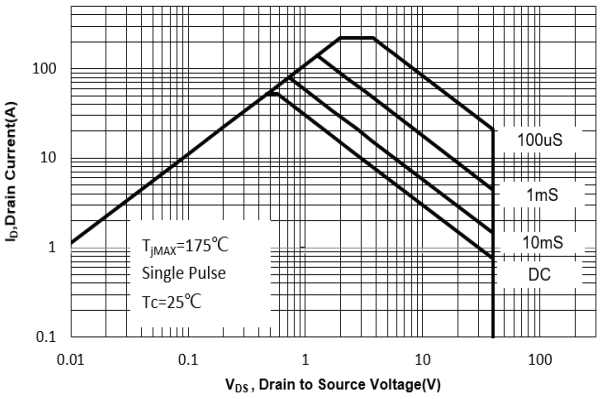


Fig. 12 Safe Operation Area



Surge Components Inc. (USA)
sales@surgecomponents.com
+1 (631) 595-1818

Surge Components EMEA (Europe)
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+44-203-983-9133

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+852-2172-7607

Electrical Characteristics Curves

Fig.13 Normalized Maximum Transient Thermal Impedance($Z_{\theta JC}$)

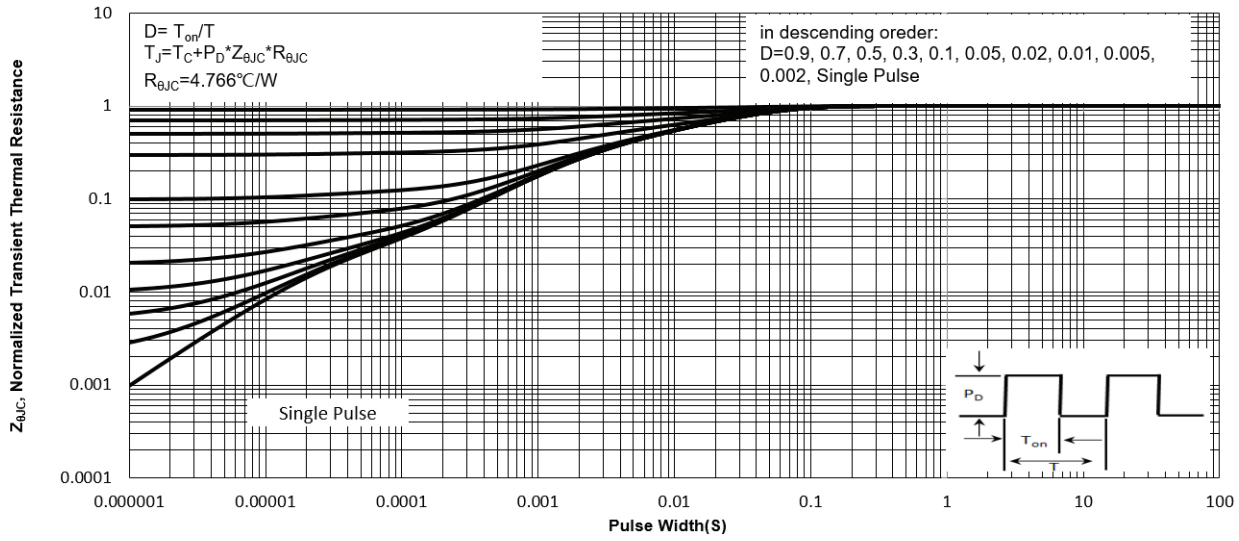
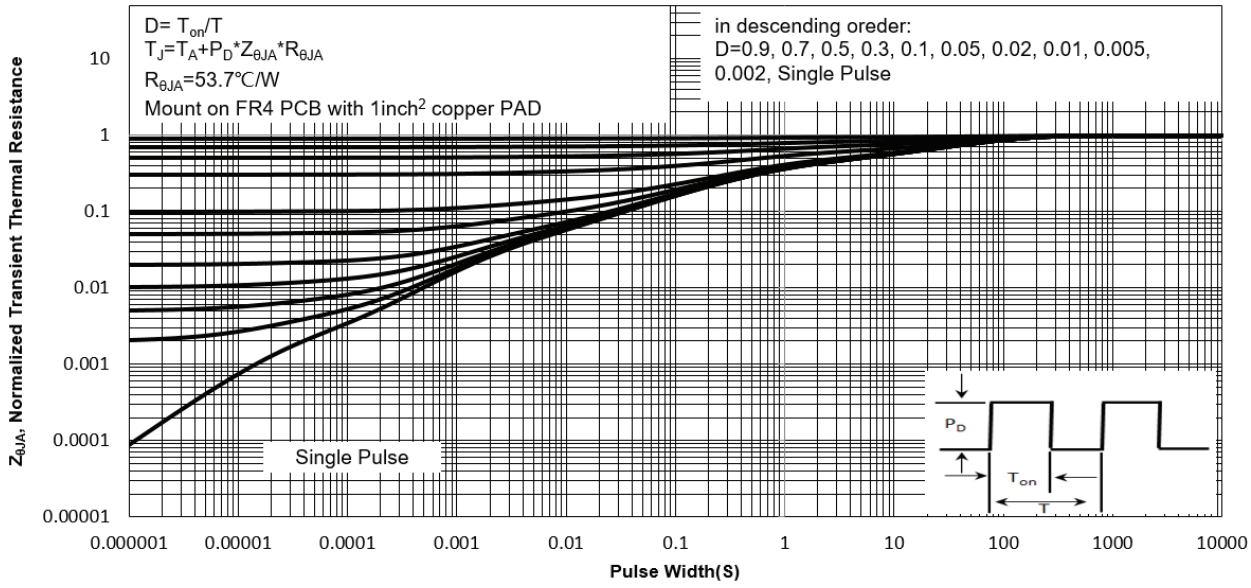


Fig.14 Normalized Maximum Transient Thermal Impedance($Z_{\theta JA}$)



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Test Circuits

Fig.1-1 Switching times test circuit

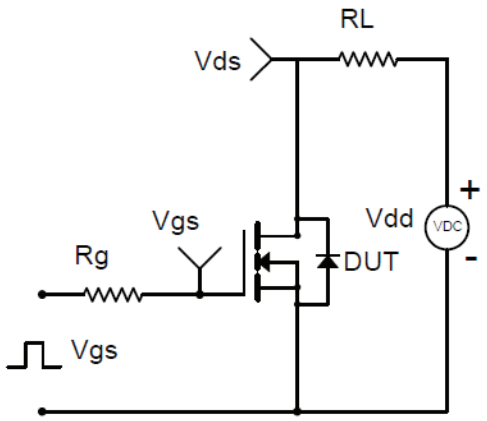


Fig.1-2 Switching Waveform

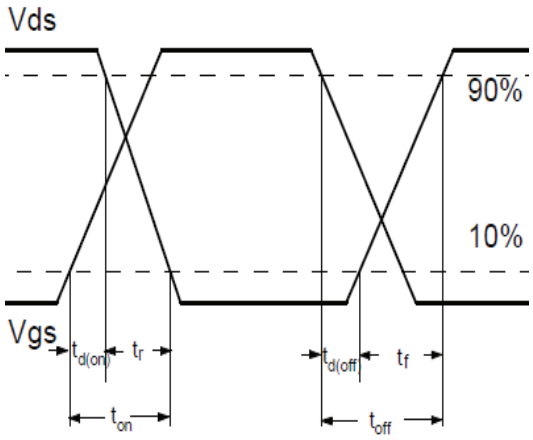


Fig.2-1 Gate charge test circuit

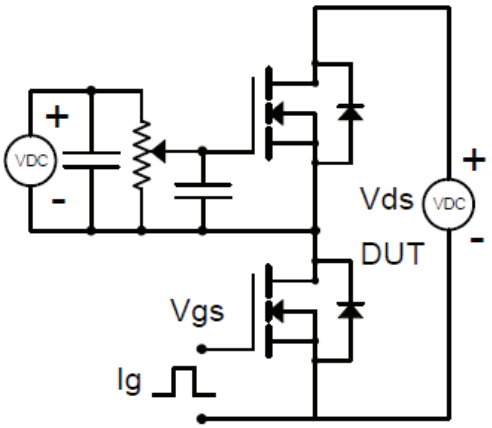


Fig.2-2 Gate charge waveform

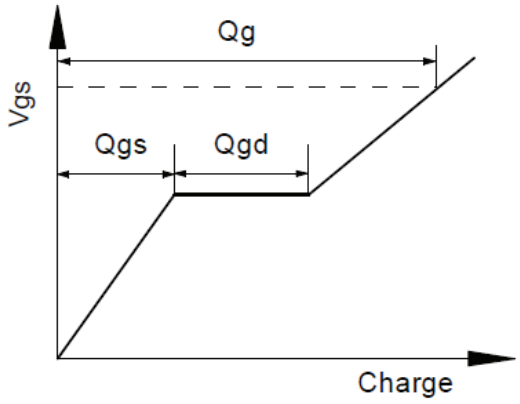


Fig.3-1 Avalanche test circuit

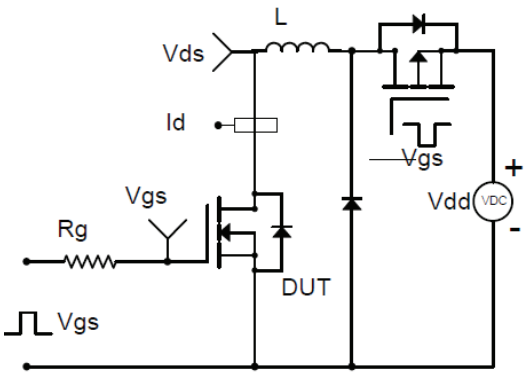
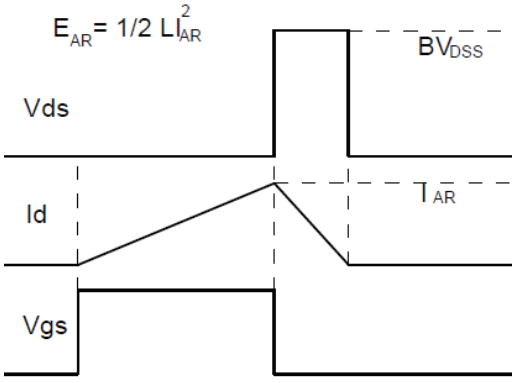


Fig.3-2 Avalanche waveform



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+44-203-983-9133

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surgehk@surgecomponents.com.hk
+852-2172-7607