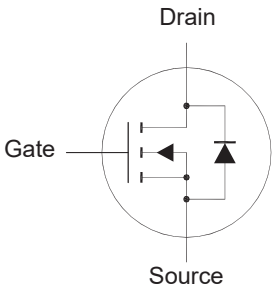
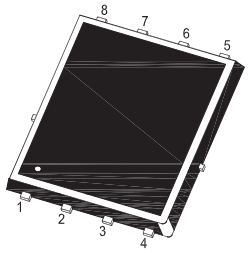
# N-Channel Enhancement Mode MOSFET

## Features

- Low $R_{DS(ON)}$
- AEC-Q101 Qualified
- Surface-mounted package
- Low Gate-Source Threshold Voltage
- Halogen and Antimony Free(HAF), RoHS compliant




1.Source 2.Source 3.Source 4.Gate
5.Drain 6.Drain 7.Drain 8.Drain
DFN5060 Plastic Package

## Key Parameters

| Parameter | Value | Unit |
|---|---|---|
| $BV_{DSS}$ | 65 | V |
| $R_{DS(ON)}$ Max | 5 @ $V_{GS}$ = 10 V | mΩ |
| | 7.5 @ $V_{GS}$ = 4.5 V | |
| $V_{GS(th)}$ typ | 1.7 | V |
| $Q_g$ typ | 38.3 @ $V_{GS}$ = 10 V | nC |

## Absolute Maximum Ratings (at $T_a$ = 25℃ unless otherwise specified)

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | 65 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 20 | V |
| Drain Current | $T_c$ = 25℃ | $I_D$ | 84 | A |
| | $T_c$ = 100℃ | | 59 | |
| Peak Drain Current, Pulsed [1] | | $I_{DM}$ | 330 | A |
| Avalanche Current | | $I_{AS}$ | 36 | A |
| Single Pulse Avalanche Energy [2] | | $E_{AS}$ | 65 | mJ |
| Total Power Dissipation | $T_c$ = 25℃ | $P_{tot}$ | 62.5 | W |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | - 55 to + 175 | ℃ |

## Thermal Characteristics

| Parameter | Symbol | Max. | Unit |
|---|---|---|---|
| Thermal Resistance from Junction to Case | $R_{\theta JC}$ | 2.4 | ℃/W |
| Thermal Resistance from Junction to Ambient [3] | $R_{\theta JA}$ | 55 | ℃/W |

[1] Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ = 175°C.

[2] Limited by $T_{J(MAX)}$, starting $T_J$ = 25 °C, L = 0.1 mH, $R_g$ = 25 Ω, $I_{AS}$ = 36 A, $V_{GS}$ = 10 V.

[3] Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.



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**Characteristics at $T_a$ = 25℃ unless otherwise specified**

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | |
| Drain-Source Breakdown Voltage<br>at $I_D$ = 1 mA | $BV_{DSS}$ | 65 | - | - | V |
| Drain-Source Leakage Current<br>at $V_{DS}$ = 52 V | $I_{DSS}$ | - | - | 1 | μA |
| Gate Leakage Current<br>at $V_{GS}$ = ± 16 V | $I_{GSS}$ | - | - | ± 100 | nA |
| Gate-Source Threshold Voltage<br>at $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | $V_{GS(th)}$ | 1.2 | - | 2.5 | V |
| Drain-Source On-State Resistance<br>at $V_{GS}$ = 10 V, $I_D$ = 20 A<br>at $V_{GS}$ = 4.5 V, $I_D$ = 15 A | $R_{DS(on)}$ | -<br>- | 4<br>- | 5<br>7.5 | mΩ |
| **DYNAMIC PARAMETERS** | | | | | |
| Forward Transconductance<br>at $V_{DS}$ = 5 V, $I_D$ = 15 A | $g_{fs}$ | - | 32 | - | S |
| Gate resistance<br>at $V_{GS}$ = 0 V, $V_{DS}$ = 0 V, f = 1 MHz | $R_g$ | - | 1 | - | Ω |
| Input Capacitance<br>at $V_{GS}$ = 0 V, $V_{DS}$ = 30 V, f = 1 MHz | $C_{iss}$ | - | 1645 | - | pF |
| Output Capacitance<br>at $V_{GS}$ = 0 V, $V_{DS}$ = 30 V, f = 1 MHz | $C_{oss}$ | - | 486 | - | pF |
| Reverse Transfer Capacitance<br>at $V_{GS}$ = 0 V, $V_{DS}$ = 30 V, f = 1 MHz | $C_{rss}$ | - | 22 | - | pF |
| Gate charge total<br>at $V_{DS}$ = 30 V, $I_D$ = 20 A, $V_{GS}$ = 10 V<br>at $V_{DS}$ = 30 V, $I_D$ = 20 A, $V_{GS}$ = 4.5 V | $Q_g$ | -<br>- | 38.3<br>20.3 | -<br>- | nC |
| Gate to Source Charge<br>at $V_{DS}$ = 30 V, $I_D$ = 20 A, $V_{GS}$ = 10 V | $Q_{gs}$ | - | 6 | - | nC |
| Gate to Drain Charge<br>at $V_{DS}$ = 30 V, $I_D$ = 20 A, $V_{GS}$ = 10 V | $Q_{gd}$ | - | 11.4 | - | nC |
| Turn-On Delay Time<br>at $V_{DD}$ = 30 V, $I_D$ = 20 A, $V_{GS}$ = 10 V, $R_g$ = 3.3 Ω | $t_{d(on)}$ | - | 15 | - | ns |
| Turn-On Rise Time<br>at $V_{DD}$ = 30 V, $I_D$ = 20 A, $V_{GS}$ = 10 V, $R_g$ = 3.3 Ω | $t_r$ | - | 26 | - | ns |
| Turn-Off Delay Time<br>at $V_{DD}$ = 30 V, $I_D$ = 20 A, $V_{GS}$ = 10 V, $R_g$ = 3.3 Ω | $t_{d(off)}$ | - | 15 | - | ns |
| Turn-Off Fall Time<br>at $V_{DD}$ = 30 V, $I_D$ = 20 A, $V_{GS}$ = 10 V, $R_g$ = 3.3 Ω | $t_f$ | - | 3 | - | ns |
| **Body-Diode PARAMETERS** | | | | | |
| Drain-Source Diode Forward Voltage<br>at $I_S$ = 1 A, $V_{GS}$ = 0 V | $V_{SD}$ | - | - | 1.3 | V |
| Body-Diode Continuous Current | $I_S$ | - | - | 84 | A |
| Body-Diode Continuous Current, Pulsed | $I_{SM}$ | - | - | 330 | A |
| Body Diode Reverse Recovery Time<br>at $I_S$ = 20 A, di/dt = 100 A / μs | $t_{rr}$ | - | 39 | - | ns |
| Body Diode Reverse Recovery Charge<br>at $I_S$ = 20 A, di/dt = 100 A / μs | $Q_{rr}$ | - | 42 | - | nC |


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## Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

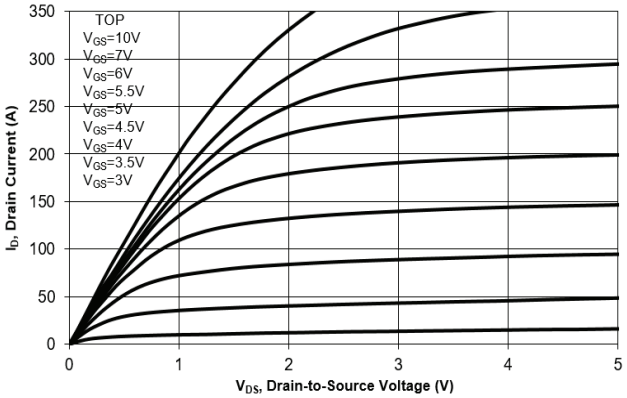



Fig. 2 Typical Transfer Characteristics

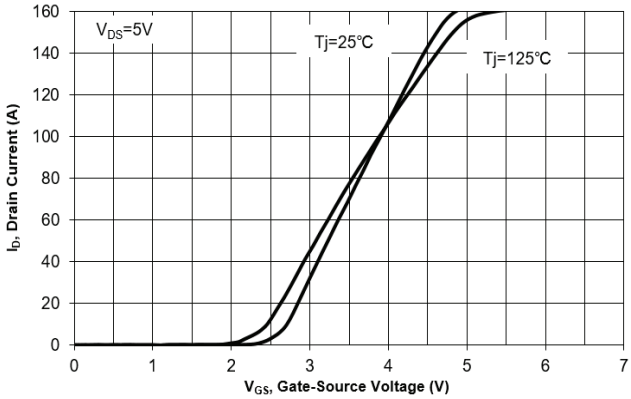



Fig. 3 On-Resistance vs. Drain Current

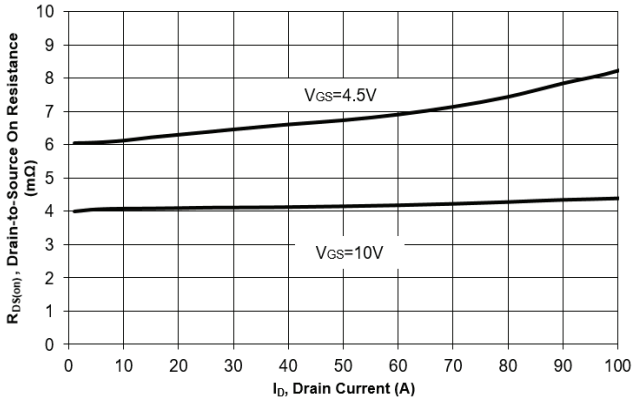



Fig. 4 On-Resistance vs. Gate to Source Voltage

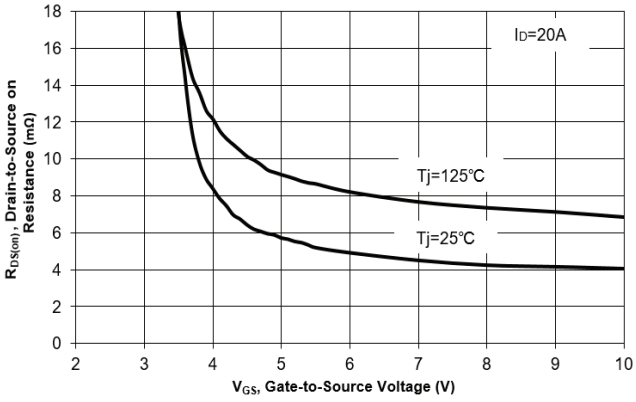



Fig. 5 On-Resistance vs.$T_j$

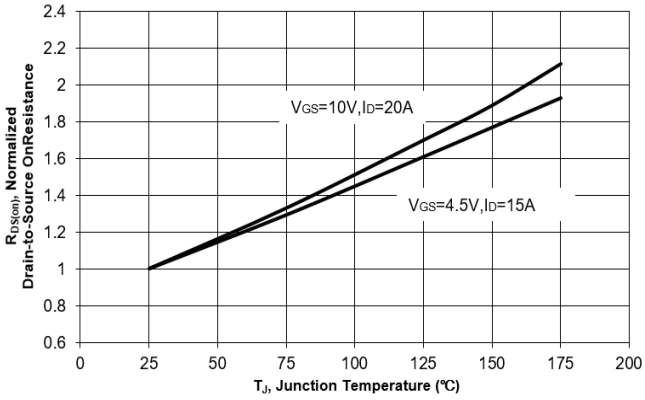
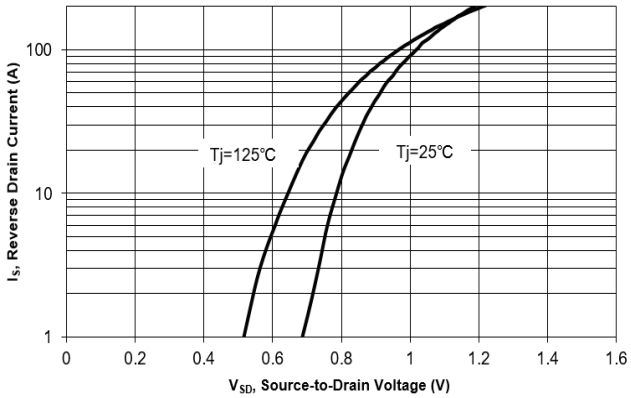



Fig. 6 Typical Body-Diode Forward Characteristics





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## Electrical Characteristics Curves

Fig. 13 Normalized Maximum Transient Thermal Impedance($z_{\Theta JC}$)

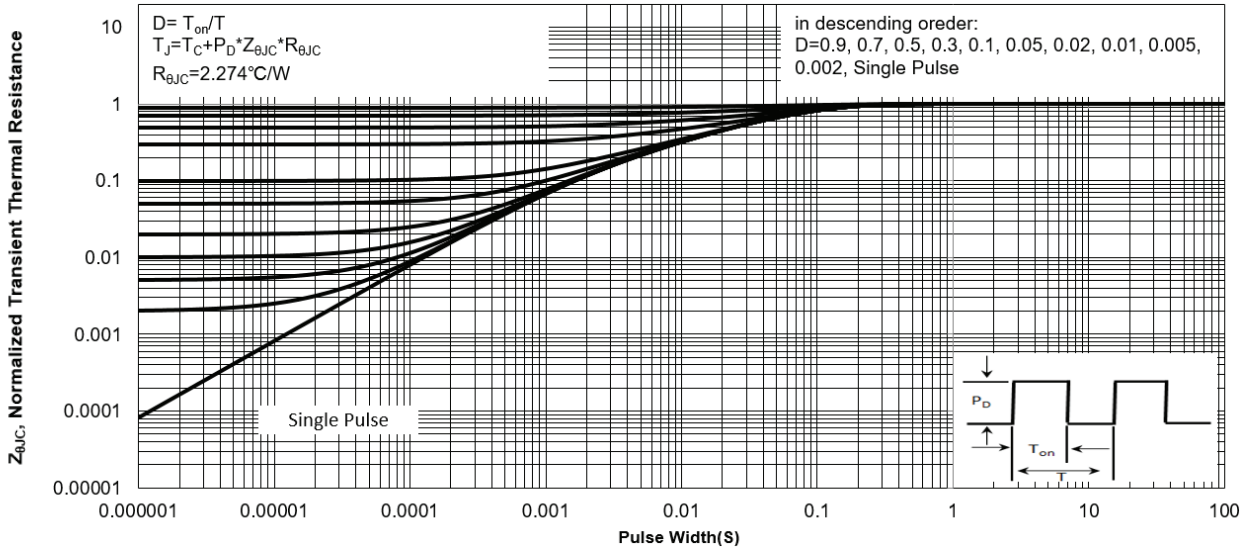
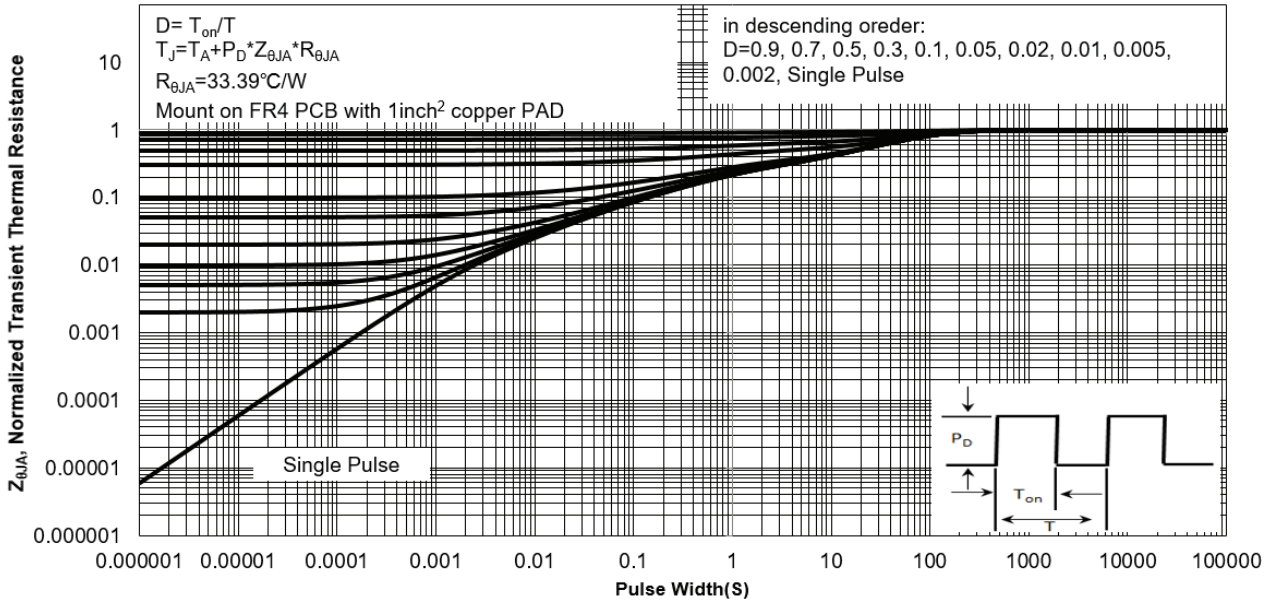



Fig. 14 Normalized Maximum Transient Thermal Impedance($z_{\Theta JA}$)





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## Test Circuits

Fig.1-1 Switching times test circuit

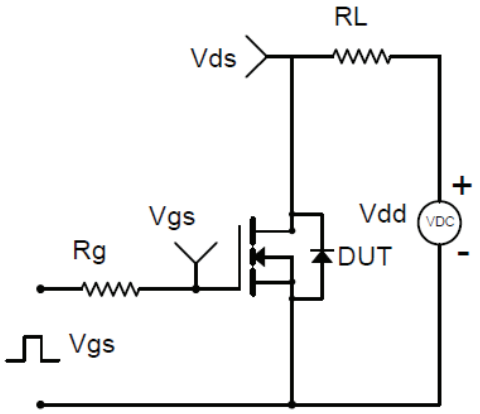



Fig.1-2 Switching Waveform

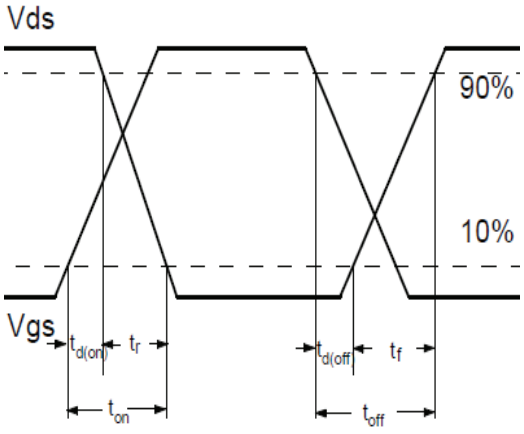



Fig.2-1 Gate charge test circuit

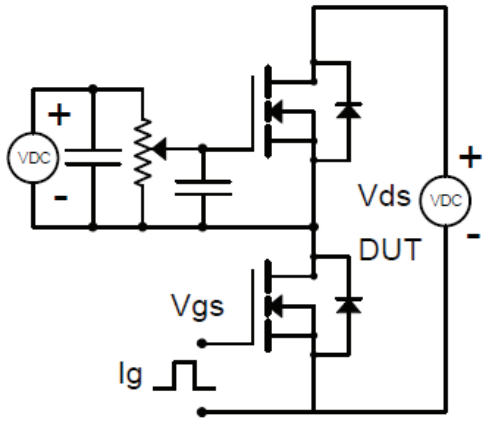



Fig.2-2 Gate charge waveform

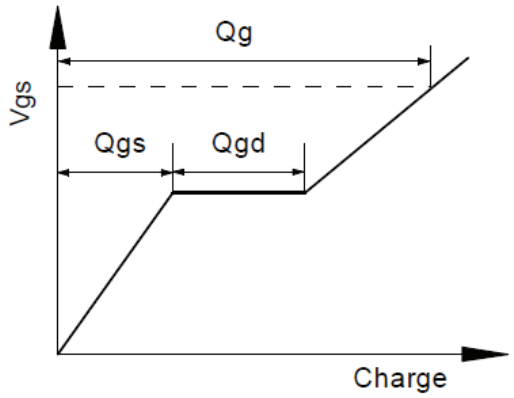



Fig.3-1 Avalanche test circuit

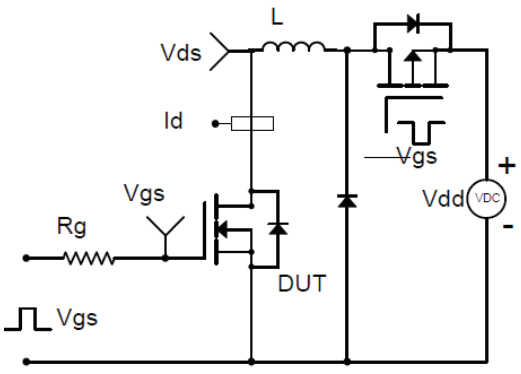
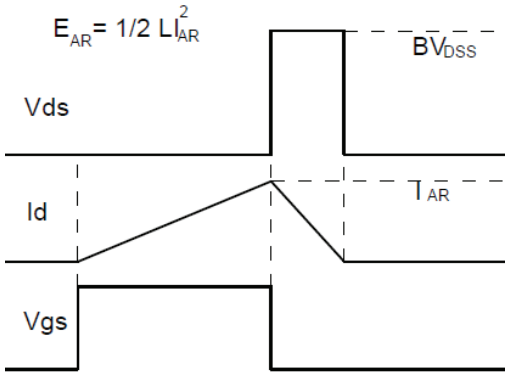



Fig.3-2 Avalanche waveform





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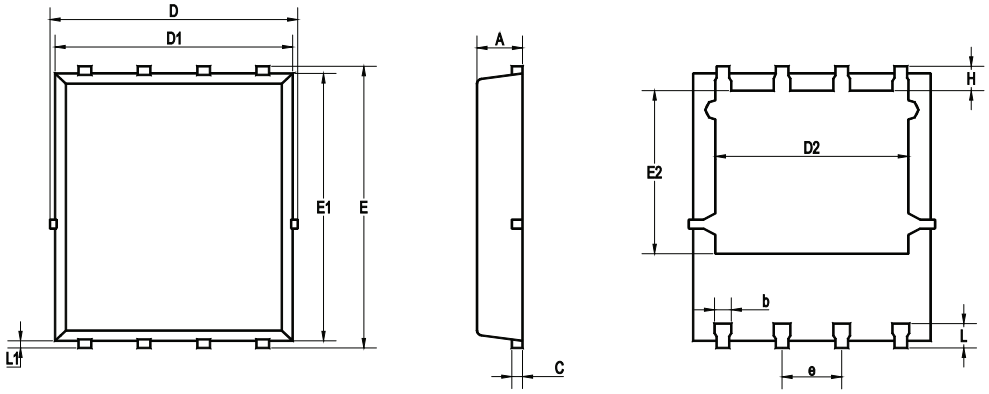
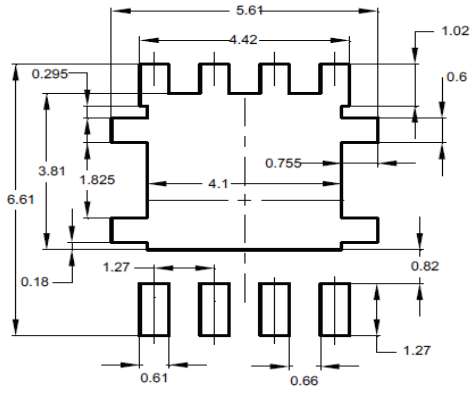
## Package Outline Dimensions (Units: mm) DFN5060




| UNIT | A | b | C | D | D1 | D2 | E | E1 | E2 | e | L | L1 | H |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.12<br>0.9 | 0.51<br>0.33 | 0.34<br>0.11 | 5.26<br>4.7 | 5.1<br>4.7 | 4.5<br>3.56 | 6.25<br>5.75 | 6<br>5.6 | 3.66<br>3.18 | 1.37<br>1.17 | 0.71<br>0.35 | 0.2<br>0.06 | 0.71<br>0.35 |

## Recommended Soldering Footprint




## Packing information

| Package | Tape Width (mm) | Pitch | | Reel Size | | Per Reel Packing Quantity |
|---|---|---|---|---|---|---|
| | | mm | inch | mm | inch | |
| DFN5060 | 12 | 8 ± 0.1 | 0.315 ± 0.004 | 330 | 13 | 5,000 |

## Marking information

" DM5E6N044LS " = Part No.
" ****** " = Date Code Marking
Font type: Arial

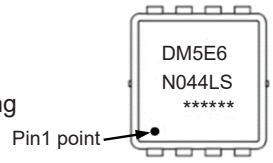



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Fig. 7 Typical Junction Capacitance

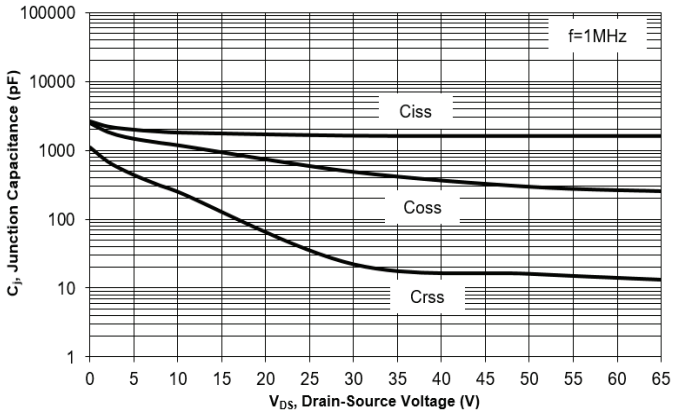



Fig. 8 Drain-Source Leakage Current vs. $T_j$

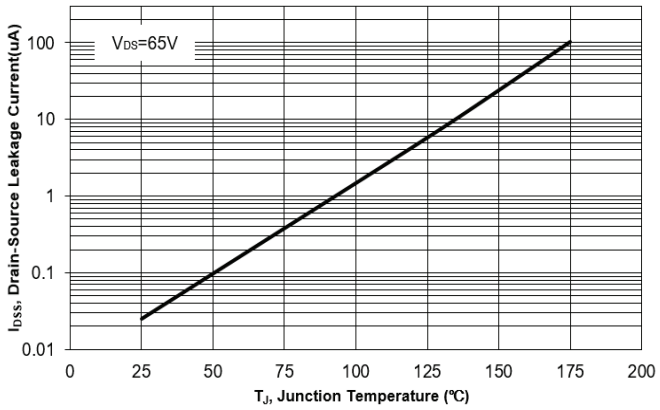



Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

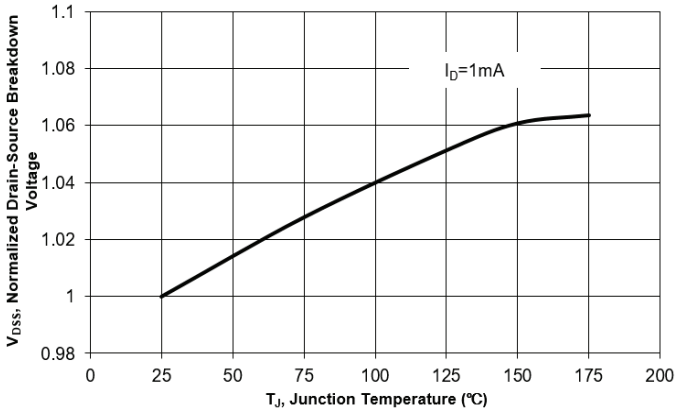



Fig. 10 Gate Threshold Variation vs. $T_j$

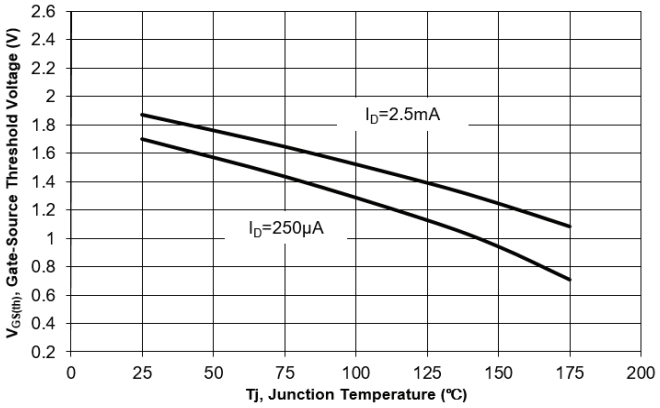



Fig. 11 Gate Charge

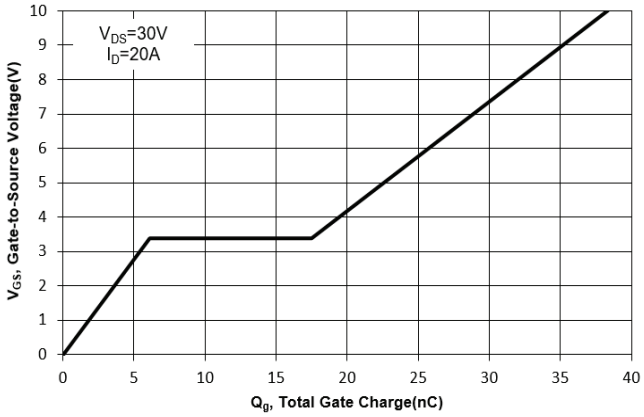
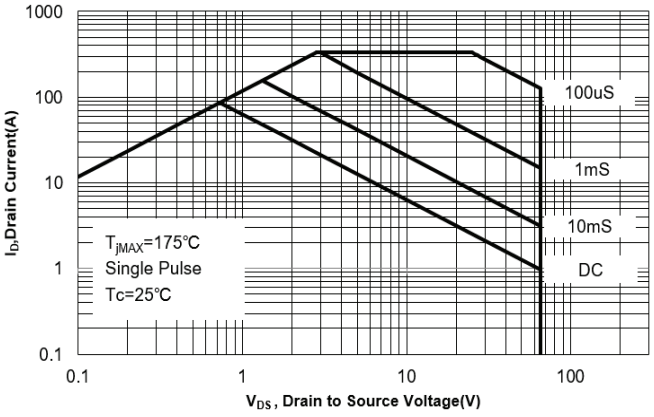



Fig. 12 Safe Operation Area



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