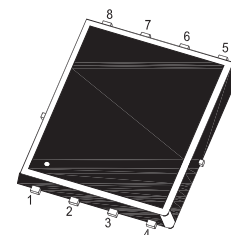
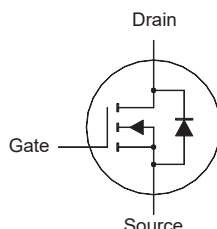


N-Channel Enhancement Mode MOSFET
Features

- AEC-Q101 Qualified
- Surface-mounted package
- Low Gate-Source Threshold Voltage
- Halogen and Antimony Free(HAF), RoHS compliant

Application

- Load switch
- PWM applications
- LCD TV CCFL inverter



1.Source 2.Source 3.Source 4.Gate
5.Drain 6.Drain 7.Drain 8.Drain
DFN5060 Plastic Package

Key Parameters

Parameter	Value	Unit
BV_{DSS}	65	V
$R_{DS(ON)}$ Max	11 @ $V_{GS} = 10\text{ V}$	m Ω
	16.5 @ $V_{GS} = 4.5\text{ V}$	
$V_{GS(th)}$ typ	1.7	V
Q_g typ	15 @ $V_{GS} = 10\text{ V}$	nC

Absolute Maximum Ratings(at $T_a = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	I_D	45	A
		28	
	$T_c = 25^\circ\text{C}$		
	$T_c = 100^\circ\text{C}$		
Peak Drain Current, Pulsed ¹⁾	I_{DM}	160	A
Avalanche Current	I_{AS}	12	A
Single Pulse Avalanche Energy ²⁾	E_{AS}	36	mJ
Power Dissipation	P_D	31.2	W
	$T_c = 25^\circ\text{C}$		
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	4	$^\circ\text{C/W}$
Thermal Resistance from Junction to Ambient ³⁾	$R_{\theta JA}$	50	$^\circ\text{C/W}$

¹⁾ Pulse Test: Pulse Width $\leq 100\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.

²⁾ Limited by $T_{J(MAX)}$, starting $T_J = 25^\circ\text{C}$, $L = 0.5\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 12\text{ A}$, $V_{GS} = 10\text{ V}$.

³⁾ Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

Characteristics at $T_a = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at $I_D = 250\ \mu\text{A}$	BV_{DSS}	65	-	-	V
Drain-Source Leakage Current at $V_{DS} = 52\ \text{V}$	I_{DSS}	-	-	1	μA
Gate Leakage Current at $V_{GS} = \pm 16\ \text{V}$	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at $V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	$V_{GS(th)}$	1.2	-	2.5	V
Drain-Source On-State Resistance at $V_{GS} = 10\ \text{V}$, $I_D = 10\ \text{A}$ at $V_{GS} = 4.5\ \text{V}$, $I_D = 8\ \text{A}$	$R_{DS(on)}$	- -	8.1 -	11 16.5	m Ω
DYNAMIC PARAMETERS					
Forward Transconductance at $V_{DS} = 5\ \text{V}$, $I_D = 5\ \text{A}$	g_{fs}	-	14	-	S
Gate Resistance at $V_{GS} = 0\ \text{V}$, $V_{DS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	R_g	-	1.3	-	Ω
Input Capacitance at $V_{GS} = 0\ \text{V}$, $V_{DS} = 30\ \text{V}$, $f = 1\ \text{MHz}$	C_{iss}	-	830	-	pF
Output Capacitance at $V_{GS} = 0\ \text{V}$, $V_{DS} = 30\ \text{V}$, $f = 1\ \text{MHz}$	C_{oss}	-	260	-	pF
Reverse Transfer Capacitance at $V_{GS} = 0\ \text{V}$, $V_{DS} = 30\ \text{V}$, $f = 1\ \text{MHz}$	C_{rss}	-	20	-	pF
Gate charge total at $V_{DS} = 30\ \text{V}$, $I_D = 10\ \text{A}$, $V_{GS} = 10\ \text{V}$ at $V_{DS} = 30\ \text{V}$, $I_D = 10\ \text{A}$, $V_{GS} = 4.5\ \text{V}$	Q_g	- -	15 7	- -	nC
Gate to Source Charge at $V_{DS} = 30\ \text{V}$, $I_D = 10\ \text{A}$, $V_{GS} = 10\ \text{V}$	Q_{gs}	-	3	-	nC
Gate to Drain Charge at $V_{DS} = 30\ \text{V}$, $I_D = 10\ \text{A}$, $V_{GS} = 10\ \text{V}$	Q_{gd}	-	3	-	nC
Turn-On Delay Time at $V_{DD} = 30\ \text{V}$, $I_D = 10\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_g = 4.7\ \Omega$	$t_{d(on)}$	-	10	-	ns
Turn-On Rise Time at $V_{DD} = 30\ \text{V}$, $I_D = 10\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_g = 4.7\ \Omega$	t_r	-	16	-	ns
Turn-Off Delay Time at $V_{DD} = 30\ \text{V}$, $I_D = 10\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_g = 4.7\ \Omega$	$t_{d(off)}$	-	9	-	ns
Turn-Off Fall Time at $V_{DD} = 30\ \text{V}$, $I_D = 10\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_g = 4.7\ \Omega$	t_f	-	2	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at $I_S = 1\ \text{A}$, $V_{GS} = 0\ \text{V}$	V_{SD}	-	-	1.2	V
Body-Diode Continuous Current	I_S	-	-	45	A
Body-Diode Continuous Current, Pulsed	I_{SM}	-	-	160	A
Body Diode Reverse Recovery Time at $I_S = 10\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	t_{rr}	-	17	-	ns
Body Diode Reverse Recovery Charge at $I_S = 10\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	Q_{rr}	-	7	-	nC

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

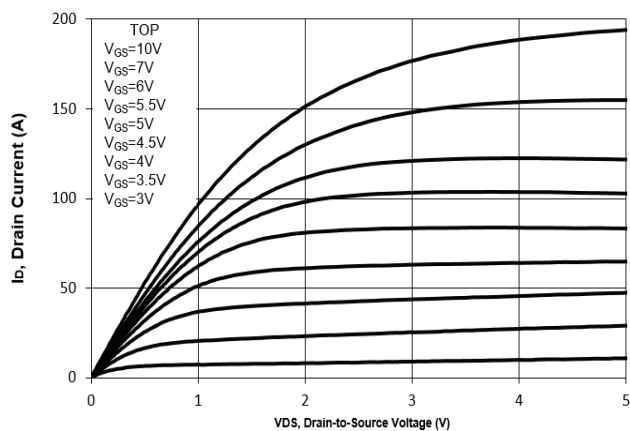


Fig. 2 Typical Transfer Characteristics

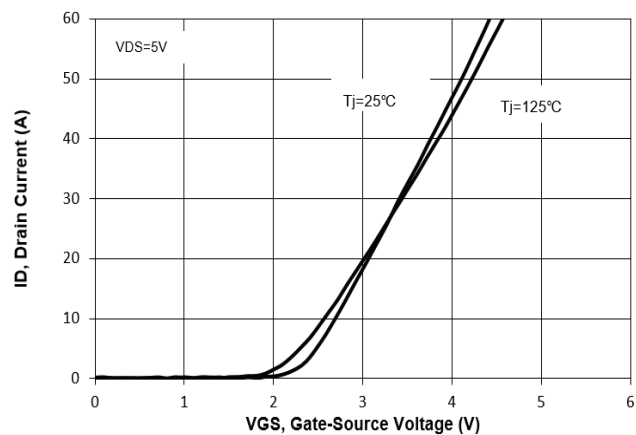


Fig. 3 on-Resistance vs. Drain Current

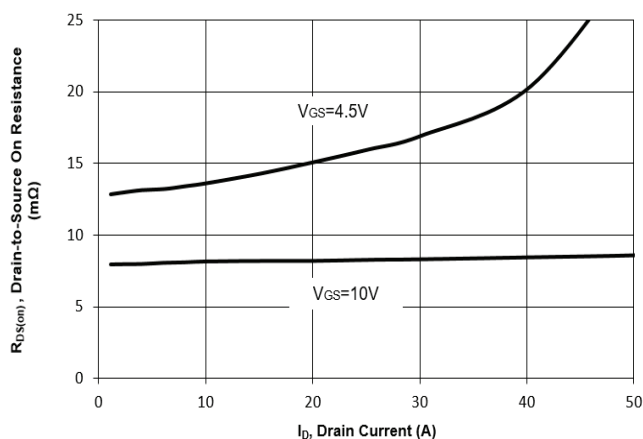


Fig. 4 on-Resistance vs. Gate to Source Voltage

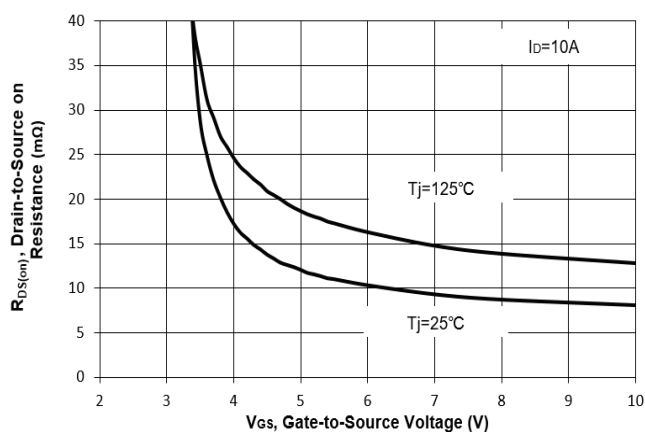


Fig. 5 on-Resistance vs. T_J

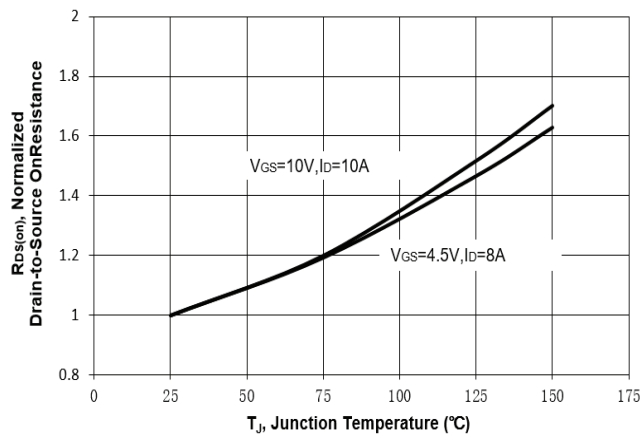
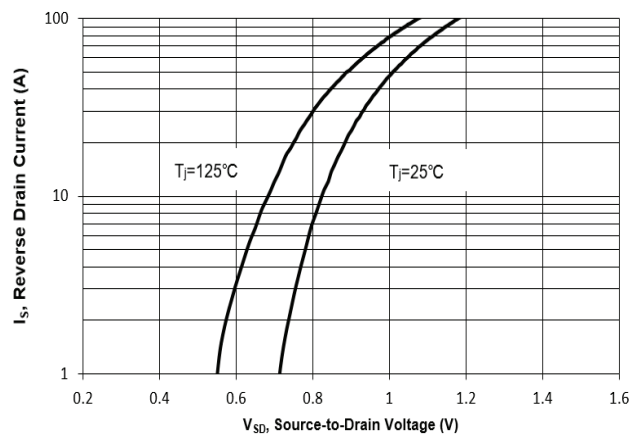


Fig. 6 Typical Body Diode Forward Characteristics



Electrical Characteristics Curves

Fig. 13 Normalized Maximum Transient Thermal Impedance($Z_{\theta JC}$)

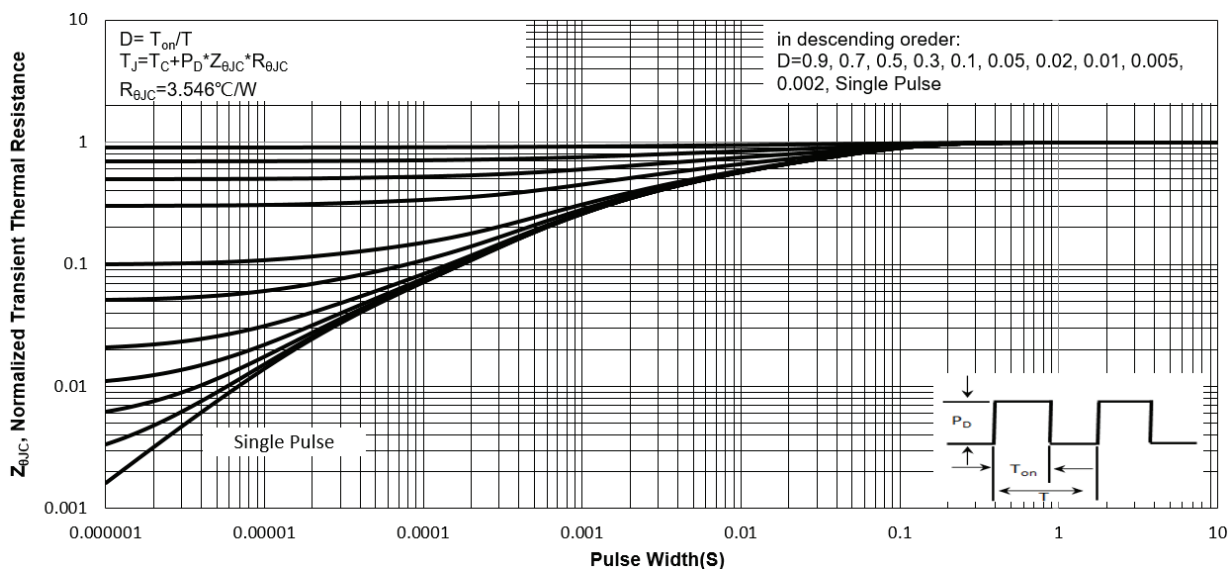
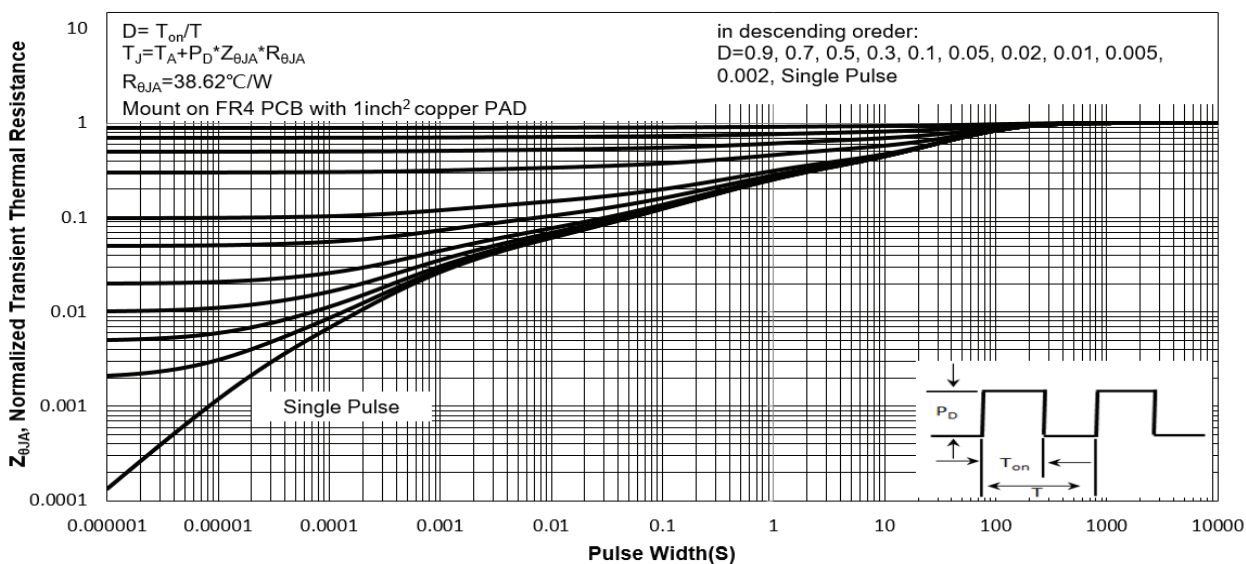


Fig. 14 Normalized Maximum Transient Thermal Impedance($Z_{\theta JA}$)



Test Circuits

Fig.1-1 Switching times test circuit

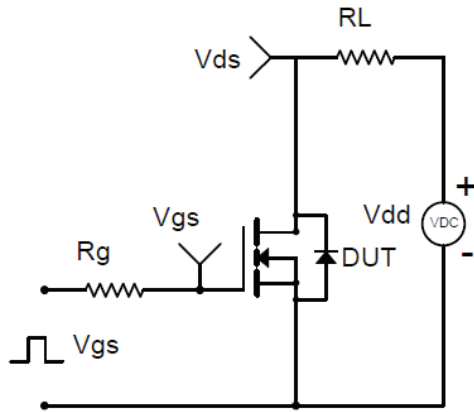


Fig.1-2 Switching Waveform

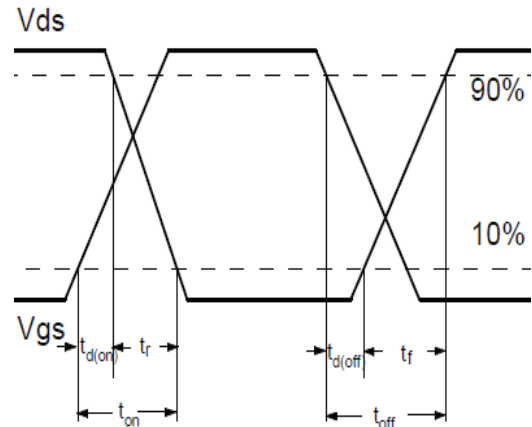


Fig.2-1 Gate charge test circuit

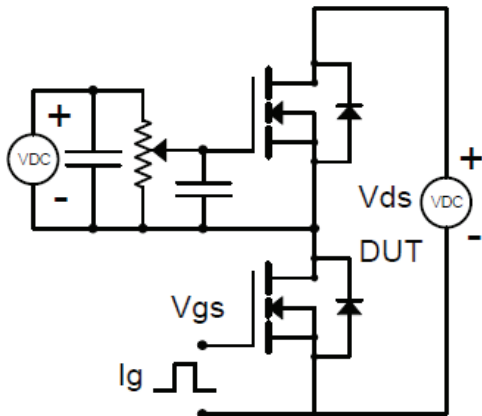


Fig.2-2 Gate charge waveform

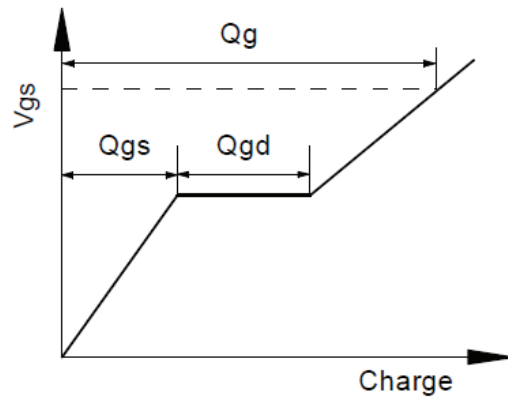


Fig.3-1 Avalanche test circuit

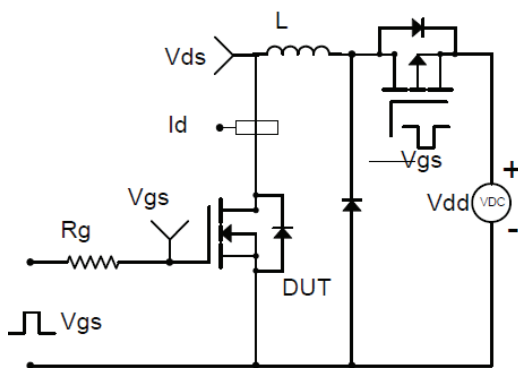
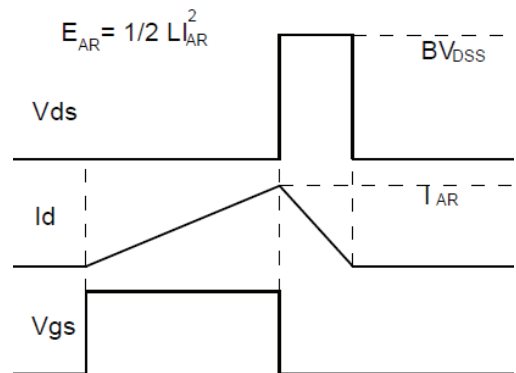
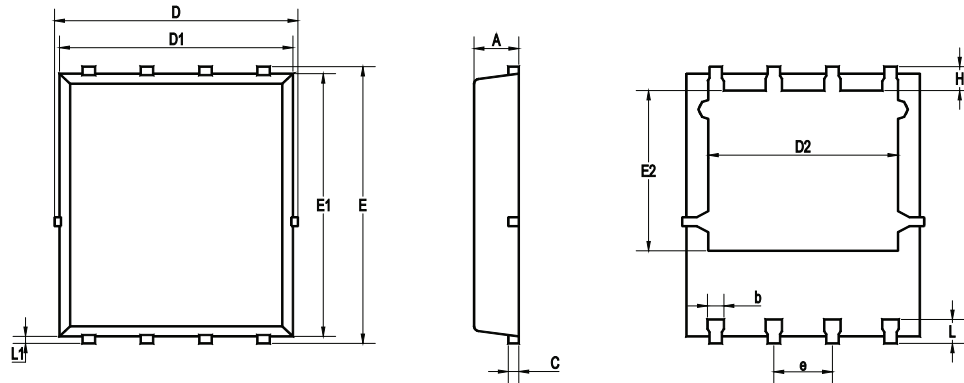


Fig.3-2 Avalanche waveform



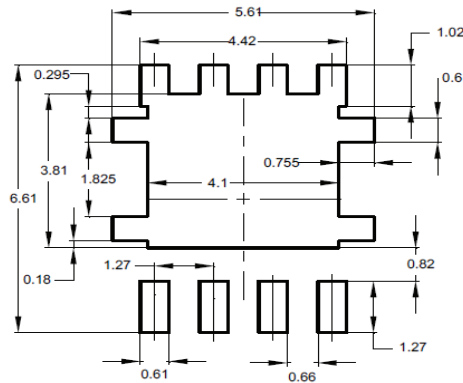
Package Outline Dimensions (Units: mm)

DFN5060



UNIT	A	b	C	D	D1	D2	E	E1	E2	e	L	L1	H
mm	1.12	0.51	0.34	5.26	5.1	4.5	6.25	6	3.66	1.37	0.71	0.2	0.71
	0.9	0.33	0.11	4.7	4.7	3.56	5.75	5.6	3.18	1.17	0.35	0.06	0.35

Recommended Soldering Footprint



Packing information

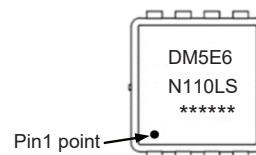
Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
DFN5060	12	8 ± 0.1	0.315 ± 0.004	330	13	5,000

Marking information

" DM5E6N110LS " = Part No.

" ***** " = Date Code Marking

Font type: Arial



Disclaimer: Our company reserves the right to make modifications, enhancements, improvements, corrections or other changes to improve product design, functions and

Fig. 7 Typical Junction Capacitance

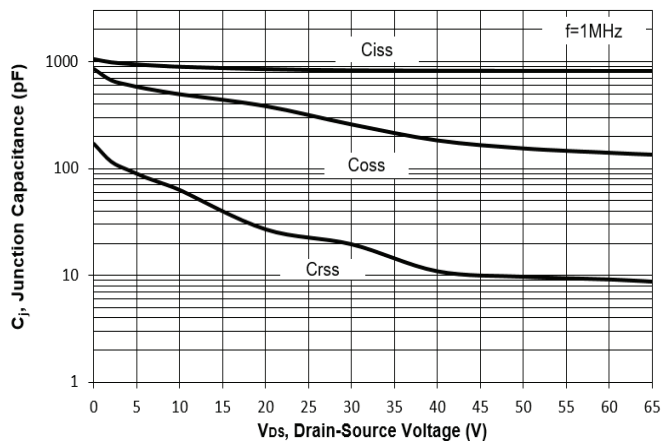


Fig. 8 Drain-Source Leakage Current vs. T_j

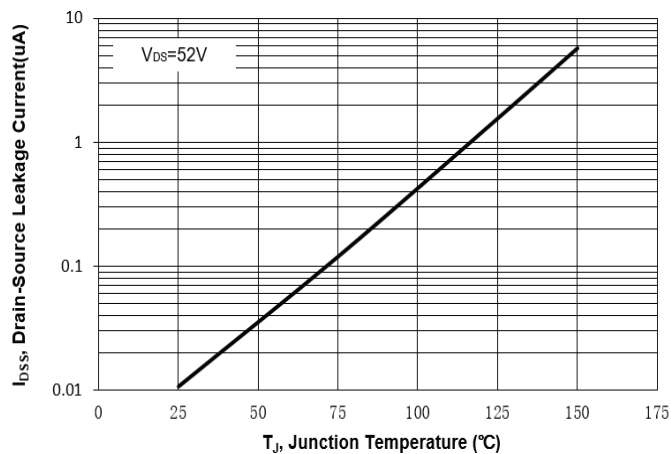


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

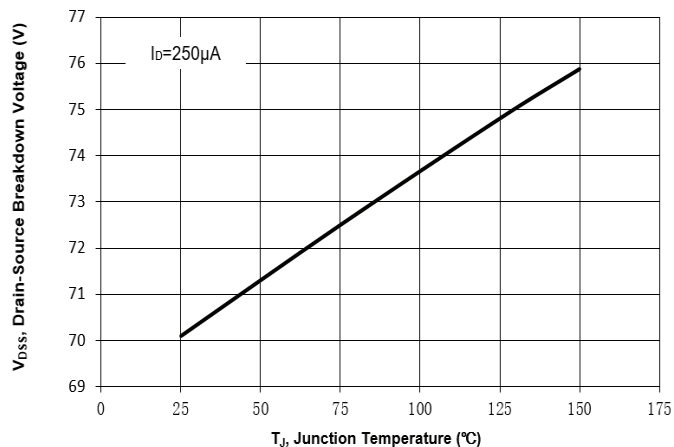


Fig. 10 Gate Threshold Variation vs. T_j

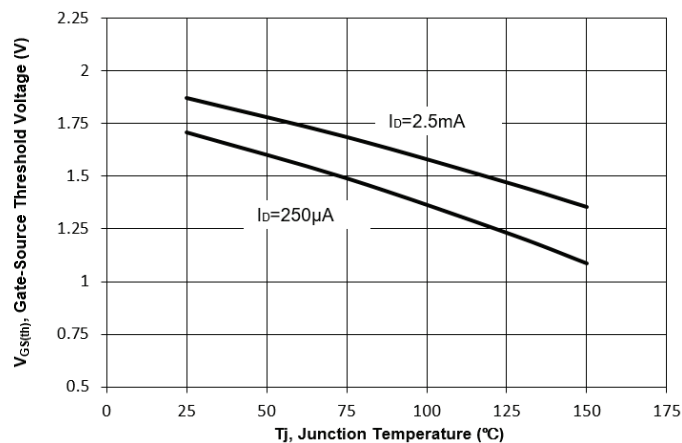


Fig. 11 Gate Charge

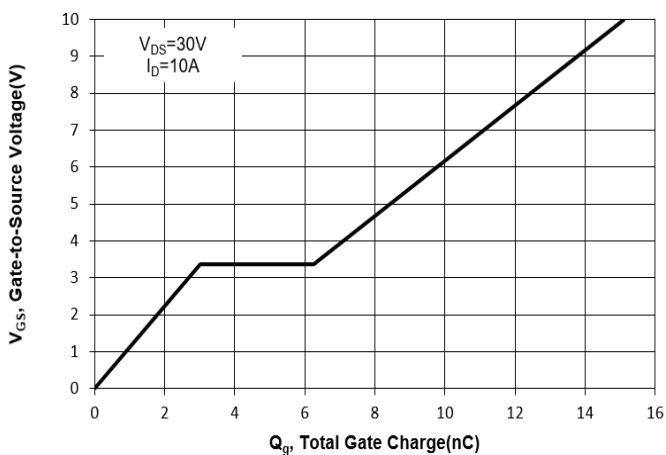


Fig. 12 Safe Operation Area

