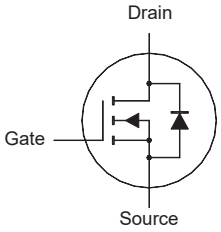
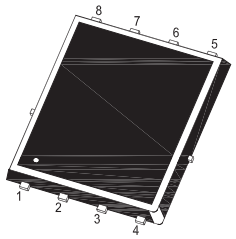
N-Channel Enhancement Mode MOSFET

Features

- AEC-Q101 Qualified
- Low Miller Capacitance
- Fully Characterized Capacitance and Avalanche
- Halogen and Antimony Free(HAF), RoHS compliant





1. Source 2. Source 3. Source 4. Gate
5. Drain 6. Drain 7. Drain 8. Drain
DFN5060 Plastic Package

Application

- BLDC Motor drive applications
- Battery powered circuits
- Synchronous rectifier applications
- Resonant mode power supplies

Key Parameters

Parameter	Value	Unit
BV_{DSS}	100	V
$R_{DS(ON)}$ Max	4.5 @ V_{GS} = 10 V	mΩ
	6.6 @ V_{GS} = 4.5 V	
$V_{GS(th)}$ typ	1.7	V
Q_g typ	75 @ V_{GS} = 10 V	nC

Absolute Maximum Ratings(at T_a = 25℃ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	T_c = 25℃	I_D	80	A
	T_c = 100℃		50	
Peak Drain Current, Pulsed [1]		I_{DM}	480	A
Single Pulse Avalanche Current		I_{AS}	24	A
Single Pulse Avalanche Energy [2]		E_{AS}	144	mJ
Power Dissipation	T_c = 25℃	P_{tot}	60	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	℃

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.5	℃/W
Thermal Resistance from Junction to Ambient [3]	$R_{\theta JA}$	50	℃/W

[1] Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ = 175°C.
[2] Limited by $T_{J(MAX)}$, starting T_J = 25 °C, L = 0.5 mH, R_g = 25 Ω, I_{AS} = 24 A, V_{GS} = 10 V.
[3] Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

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Characteristics at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I_D = 1 mA	BV_{DSS}	100	-	-	V
Drain-Source Leakage Current at V_{DS} = 80 V	I_{DSS}	-	-	1	μA
Gate Leakage Current at V_{GS} = ± 20 V	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 μA	$V_{GS(th)}$	1.2	-	2.4	V
Drain-Source On-State Resistance at V_{GS} = 10 V, I_D = 50 A at V_{GS} = 4.5 V, I_D = 20 A	$R_{DS(on)}$	- -	3.5 -	4.5 6.6	mΩ
DYNAMIC PARAMETERS					
Forward Transconductance at V_{DS} = 5 V, I_D = 30 A	g_{fs}	-	104	-	S
Gate Resistance at V_{GS} = 0 V, V_{DS} = 0 V, f = 1 MHz	R_g	-	1	-	Ω
Input Capacitance at V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	C_{iss}	-	3742	-	pF
Output Capacitance at V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	C_{oss}	-	698	-	pF
Reverse Transfer Capacitance at V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	C_{rss}	-	34	-	pF
Gate charge total at V_{DS} = 50 V, I_D = 50 A, V_{GS} = 10 V at V_{DS} = 50 V, I_D = 50 A, V_{GS} = 4.5 V	Q_g	- -	75 40	- -	nC
Gate to Source Charge at V_{DS} = 50 V, I_D = 50 A, V_{GS} = 10 V	Q_{gs}	-	14	-	nC
Gate to Drain Charge at V_{DS} = 50 V, I_D = 50 A, V_{GS} = 10 V	Q_{gd}	-	22	-	nC
Turn-On Delay Time at V_{DS} = 50 V, I_D = 50 A, V_{GS} = 10 V, R_g = 3.3 Ω	$t_{d(on)}$	-	26	-	ns
Turn-On Rise Time at V_{DS} = 50 V, I_D = 50 A, V_{GS} = 10 V, R_g = 3.3 Ω	t_r	-	43	-	ns
Turn-Off Delay Time at V_{DS} = 50 V, I_D = 50 A, V_{GS} = 10 V, R_g = 3.3 Ω	$t_{d(off)}$	-	23	-	ns
Turn-Off Fall Time at V_{DS} = 50 V, I_D = 50 A, V_{GS} = 10 V, R_g = 3.3 Ω	t_f	-	8	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I_S = 50 A, V_{GS} = 0 V	V_{SD}	-	-	1.3	V
Body-Diode Continuous Current	I_S	-	-	80	A
Body-Diode Continuous Current, Pulsed	I_{SM}	-	-	480	A
Body Diode Reverse Recovery Time at I_S = 50 A, V_{DD} = 50 V, di/dt = 200 A / μs	t_{rr}	-	48	-	ns
Body Diode Reverse Recovery Charge at I_S = 50 A, V_{DD} = 50 V, di/dt = 200 A / μs	Q_{rr}	-	106	-	nC

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Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

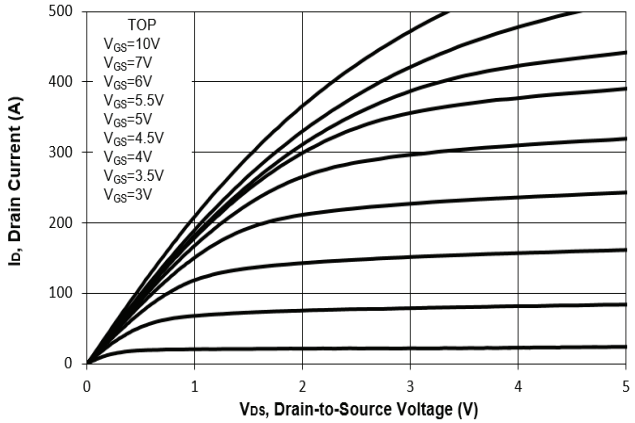

Fig. 2 Typical Transfer Characteristics

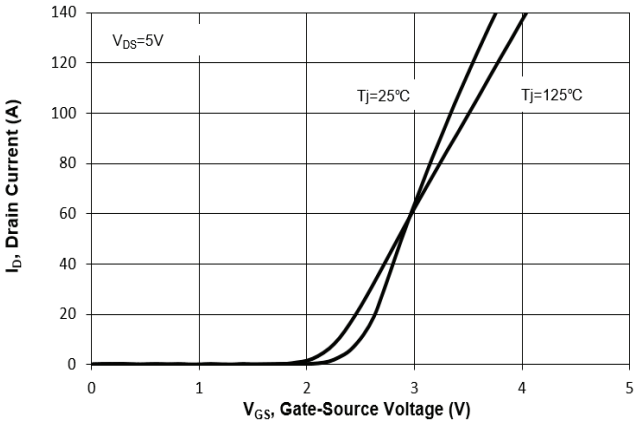

Fig. 3 on-Resistance vs. Drain Current

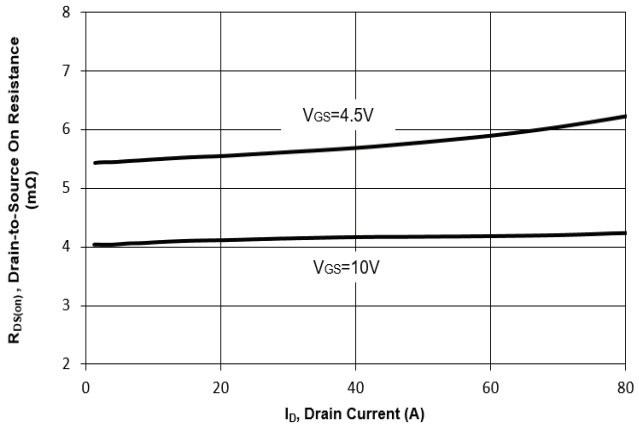

Fig. 4 on-Resistance vs. Gate to Source Voltage

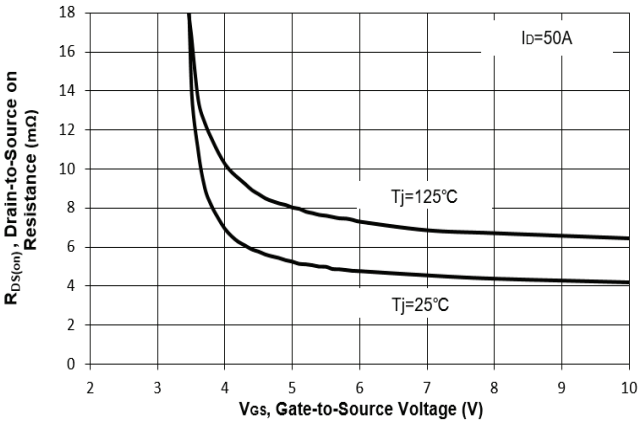

Fig. 5 on-Resistance vs.T_j

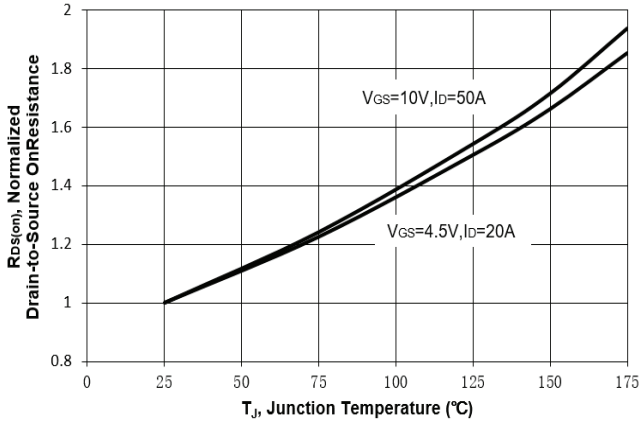

Fig. 6 Typical Body-Diode Forward Characteristics

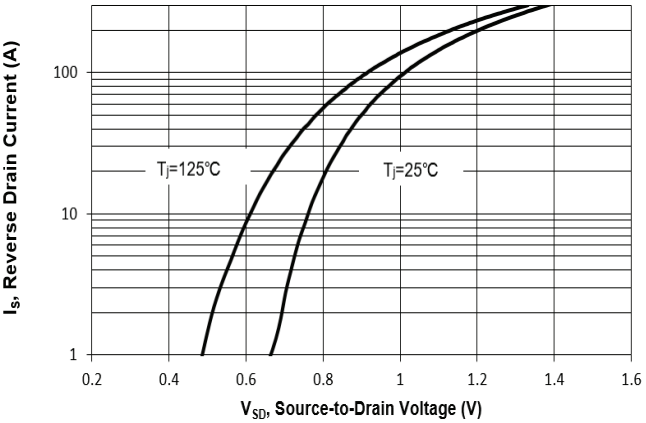

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Fig. 7 Typical Junction Capacitance

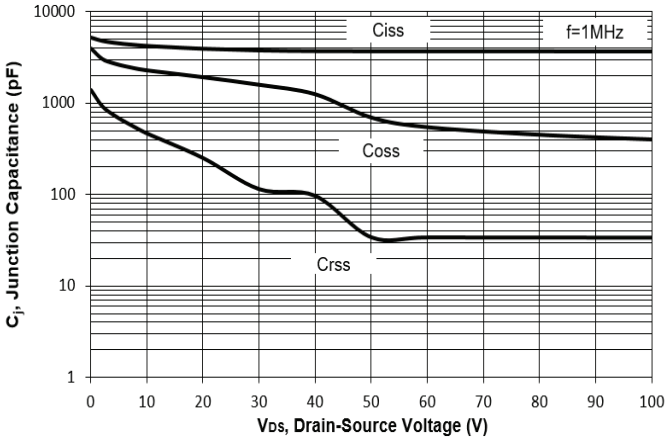


Fig. 8 Drain-Source Leakage Current vs. T_j

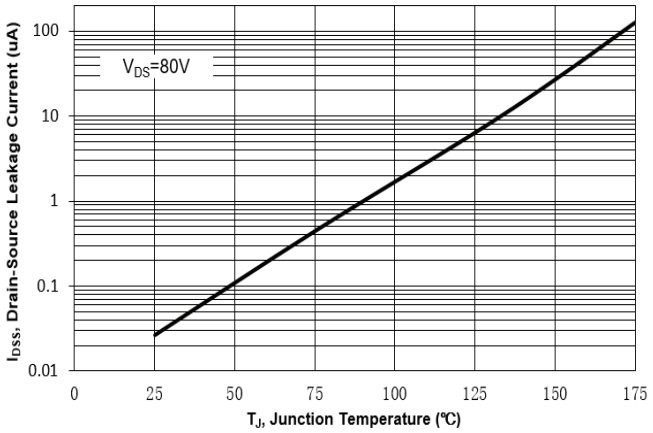


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

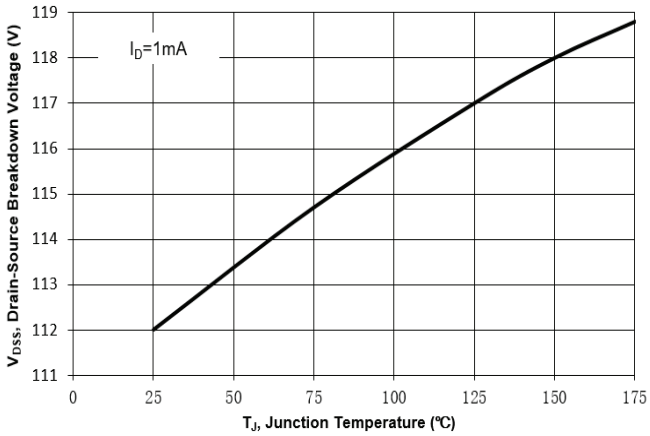


Fig. 10 Gate Threshold Variation vs. T_j

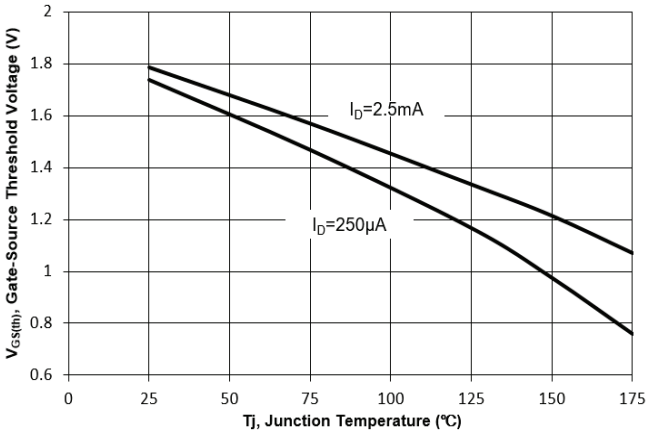


Fig. 11 Gate Charge

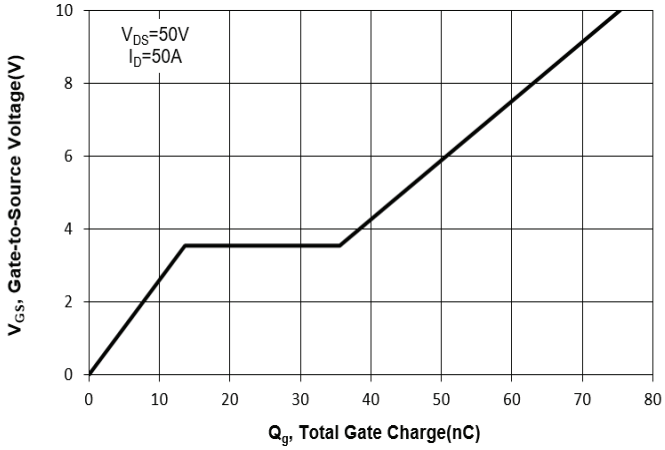
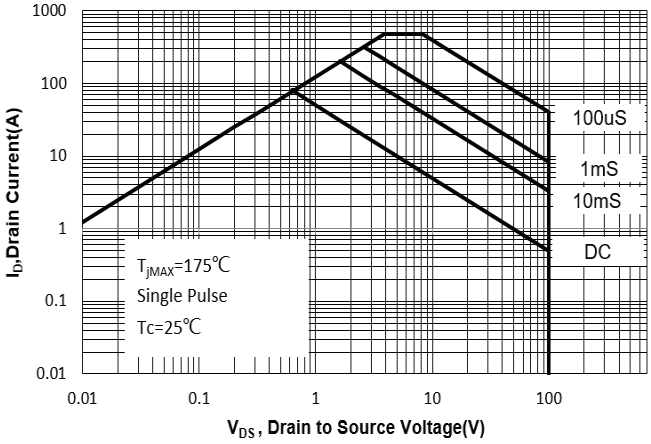


Fig. 12 Safe Operation Area



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Electrical Characteristics Curves

Fig.13 Normalized Maximum Transient Thermal Impedance($z_{\Theta JC}$)

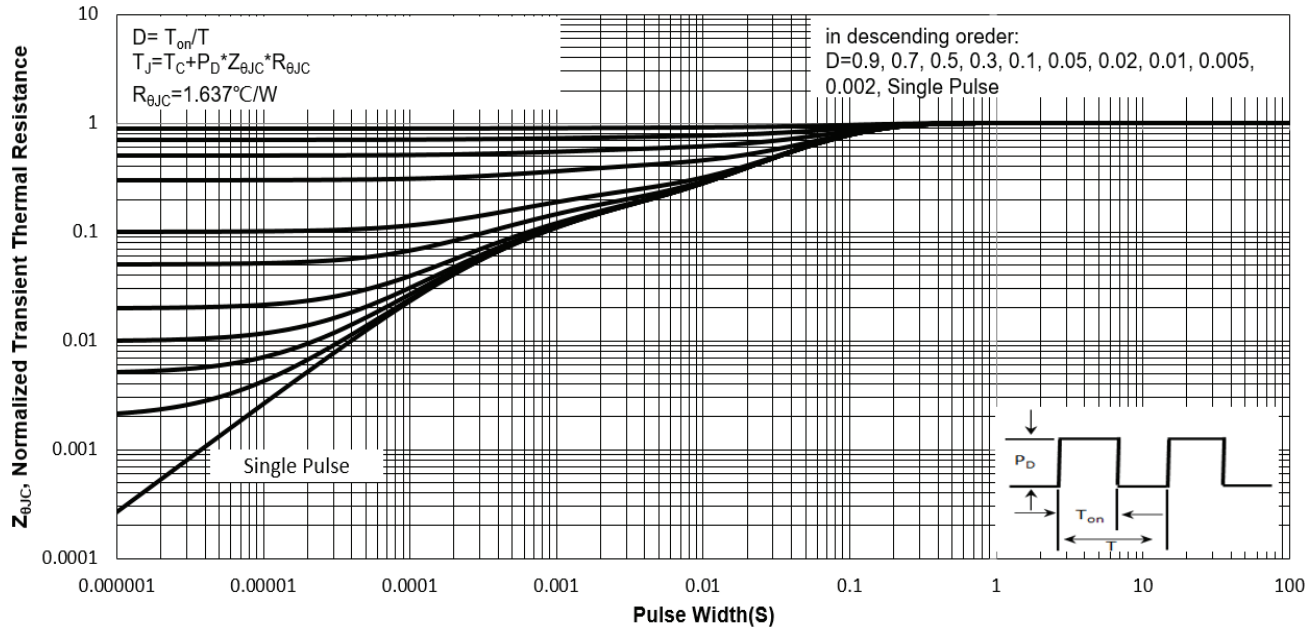
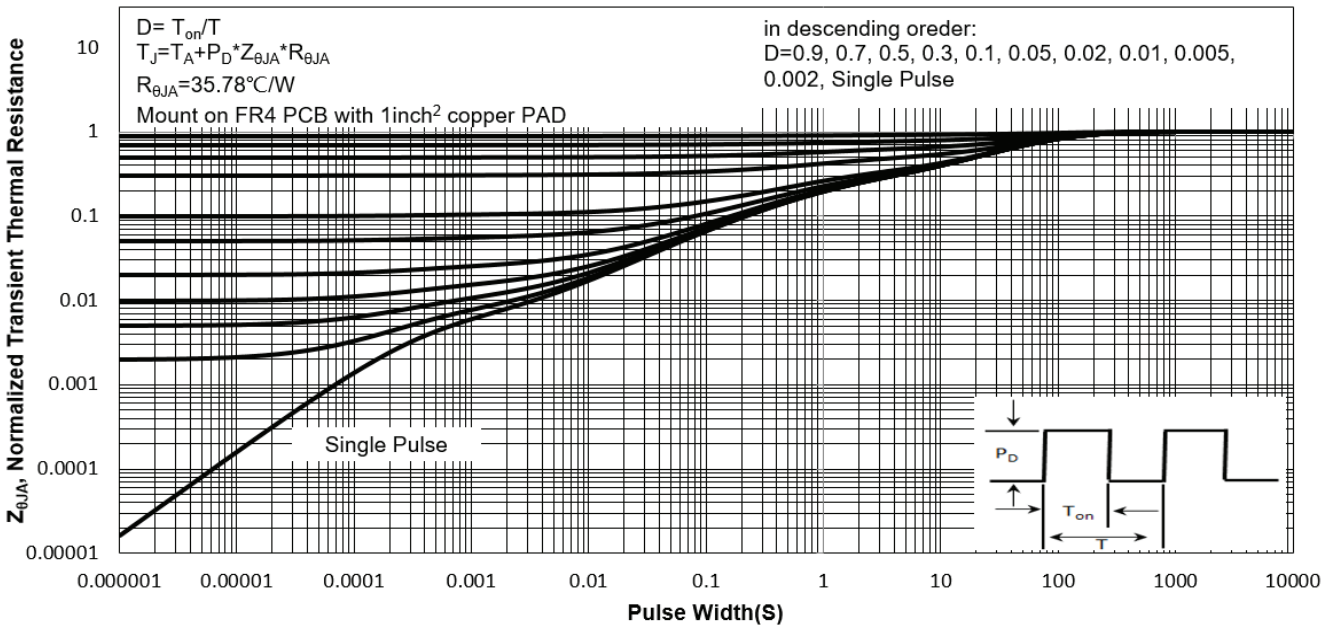


Fig.14 Normalized Maximum Transient Thermal Impedance($z_{\Theta JA}$)



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Test Circuits

Fig.1-1 Switching times test circuit

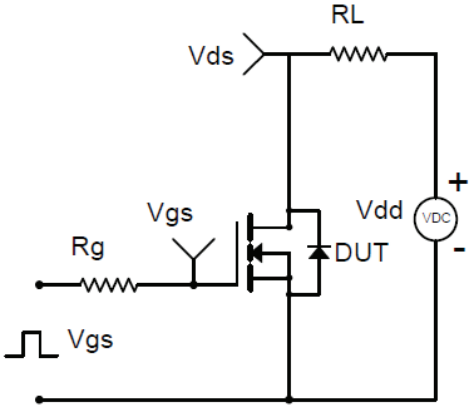


Fig.1-2 Switching Waveform

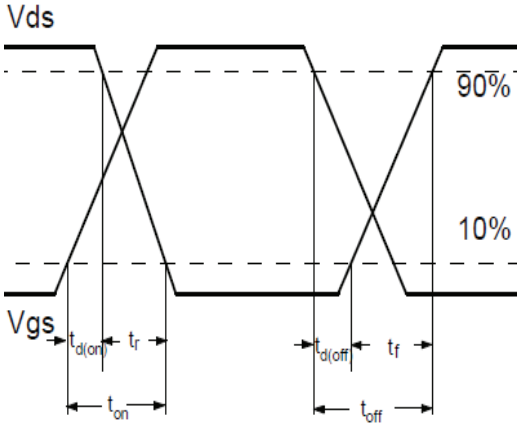


Fig.2-1 Gate charge test circuit

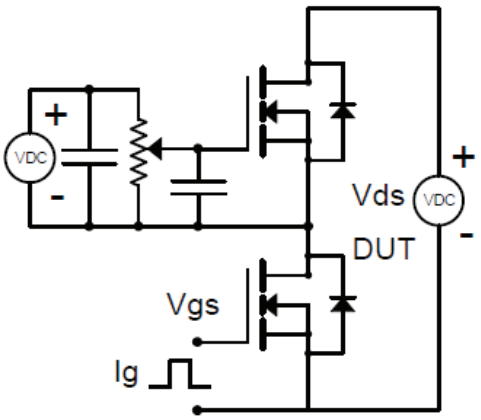


Fig.2-2 Gate charge waveform

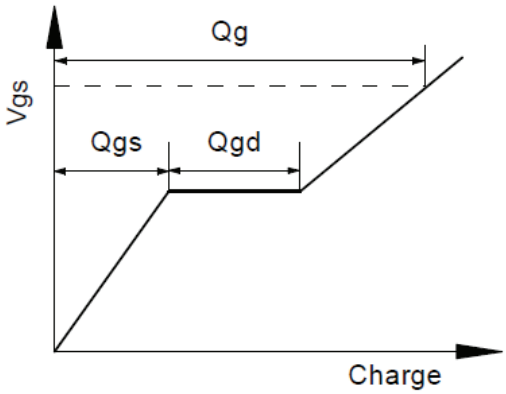


Fig.3-1 Avalanche test circuit

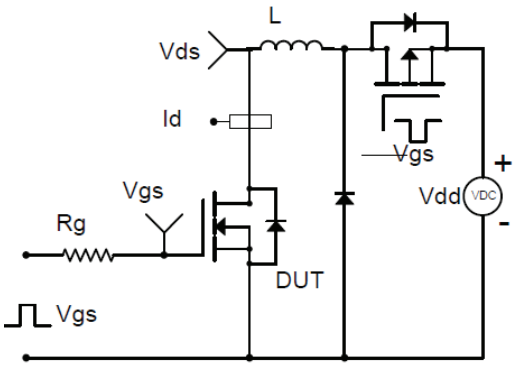
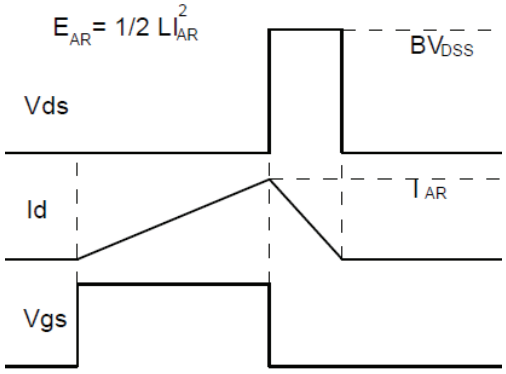


Fig.3-2 Avalanche waveform



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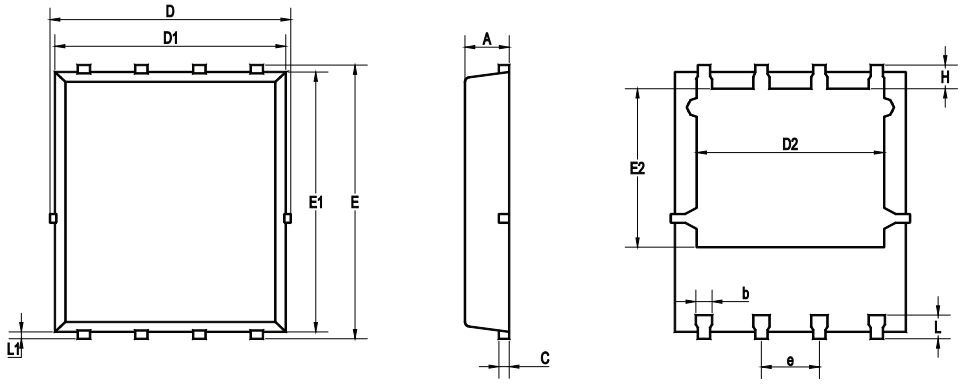
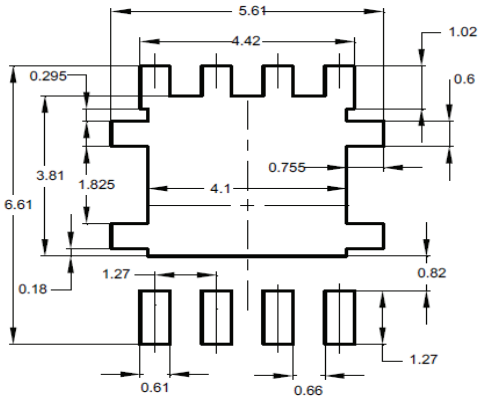
Package Outline Dimensions (Units: mm)

DFN5060



UNIT	A	b	C	D	D1	D2	E	E1	E2	e	L	L1	H
mm	1.12	0.51	0.34	5.26	5.1	4.5	6.25	6	3.66	1.37	0.71	0.2	0.71
	0.9	0.33	0.11	4.7	4.7	3.56	5.75	5.6	3.18	1.17	0.35	0.06	0.35

Recommended Soldering Footprint

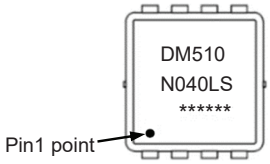


Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
DFN5060	12	8 ± 0.1	0.315 ± 0.004	330	13	5,000

Marking information

" DM510N040LS " = Part No.
" ****** " = Date Code Marking
Font type: Arial



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