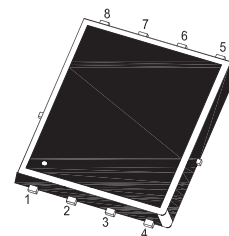
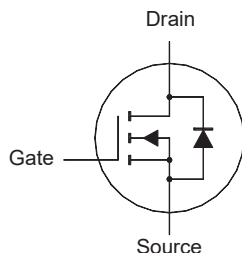


N-Channel Enhancement Mode MOSFET

Features

- AEC-Q101 Qualified
- Surface-mounted package
- Halogen and Antimony Free(HAF), RoHS compliant



1.Source 2.Source 3.Source 4.Gate
5.Drain 6.Drain 7.Drain 8.Drain
DFN5060 Plastic Package

Absolute Maximum Ratings (at $T_a = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	200	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	22	A
$T_c = 25^\circ\text{C}$		13	
$T_c = 100^\circ\text{C}$			
Peak Drain Current, Pulsed ¹⁾	I_{DM}	80	A
Single Pulse Avalanche Current	I_{AS}	18	A
Single Pulse Avalanche Energy ²⁾	E_{AS}	82.8	mJ
Total Power Dissipation	P_{tot}	59.5	W
$T_c = 25^\circ\text{C}$			
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.1	$^\circ\text{C/W}$
Thermal Resistance from Junction to Ambient ³⁾	$R_{\theta JA}$	40	$^\circ\text{C/W}$

¹⁾ Pulse Test: Pulse Width $\leq 100 \mu\text{s}$, Duty Cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.

²⁾ Limited by $T_{J(MAX)}$, starting $T_J = 25^\circ\text{C}$, $L = 0.5 \text{ mH}$, $R_g = 25 \Omega$, $I_{AS} = 18 \text{ A}$, $V_{GS} = 10 \text{ V}$.

³⁾ Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

Characteristics at $T_a = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at $I_D = 1\text{ mA}$	BV_{DSS}	200	-	-	V
Drain-Source Leakage Current at $V_{DS} = 160\text{ V}$	I_{DSS}	-	-	1	μA
Gate Leakage Current at $V_{GS} = \pm 16\text{ V}$	I_{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	$V_{GS(th)}$	2	-	4	V
Drain-Source On-State Resistance at $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$	$R_{DS(on)}$	-	42	50	m Ω
DYNAMIC PARAMETERS					
Forward Transconductance at $V_{DS} = 10\text{ V}$, $I_D = 20\text{ A}$	g_{fs}	-	19.8	-	S
Gate resistance at $V_{DS} = 0\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	R_g	-	4.3	-	Ω
Input Capacitance at $V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	C_{iss}	-	1100	-	pF
Output Capacitance at $V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	C_{oss}	-	101	-	pF
Reverse Transfer Capacitance at $V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	C_{rss}	-	10	-	pF
Gate charge total at $V_{DS} = 100\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$	Q_g	-	15.9	-	nC
Gate to Source Charge at $V_{DS} = 100\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$	Q_{gs}	-	6.8	-	nC
Gate to Drain Charge at $V_{DS} = 100\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$	Q_{gd}	-	2.7	-	nC
Turn-On Delay Time at $V_{DS} = 100\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$, $R_g = 3.3\text{ }\Omega$	$t_{d(on)}$	-	10	-	ns
Turn-On Rise Time at $V_{DS} = 100\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$, $R_g = 3.3\text{ }\Omega$	t_r	-	12	-	ns
Turn-Off Delay Time at $V_{DS} = 100\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$, $R_g = 3.3\text{ }\Omega$	$t_{d(off)}$	-	11	-	ns
Turn-Off Fall Time at $V_{DS} = 100\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$, $R_g = 3.3\text{ }\Omega$	t_f	-	2.5	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at $I_S = 1\text{ A}$, $V_{GS} = 0\text{ V}$	V_{SD}	-	-	1.2	V
Body-Diode Continuous Current	I_S	-	-	22	A
Body-Diode Continuous Current, Pulsed	I_{SM}	-	-	80	A
Body Diode Reverse Recovery Time at $I_S = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	t_{rr}	-	101	-	ns
Body Diode Reverse Recovery Charge at $I_S = 20\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	Q_{rr}	-	401	-	nC

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

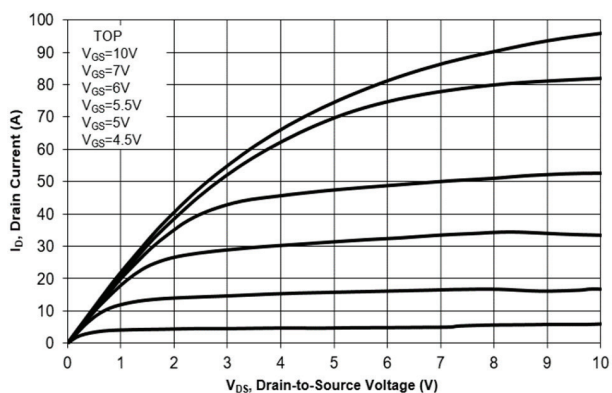


Fig. 2 Typical Transfer Characteristics

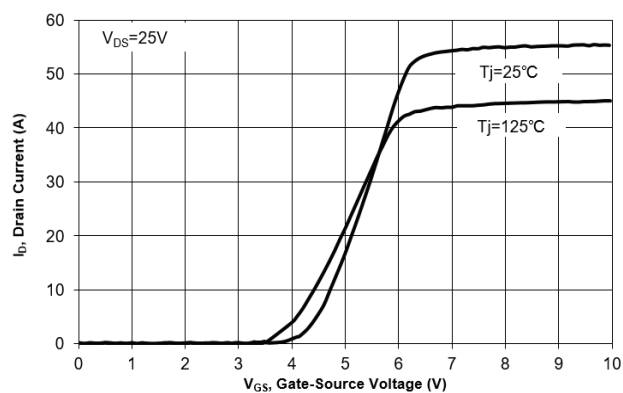


Fig. 3 On-Resistance vs. Drain Current

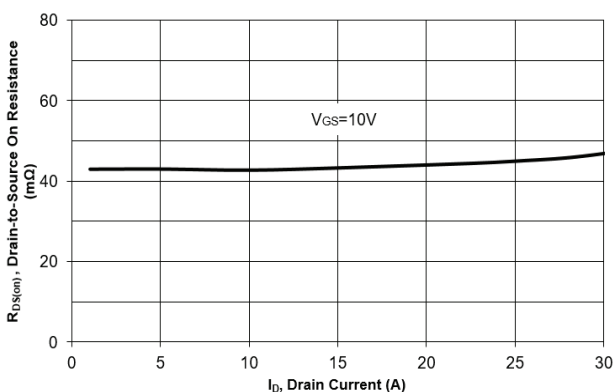


Fig. 4 On-Resistance vs. Gate to Source Voltage

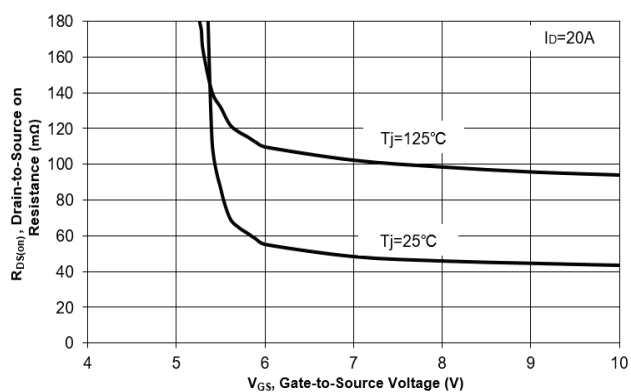


Fig. 5 On-Resistance vs. T_J

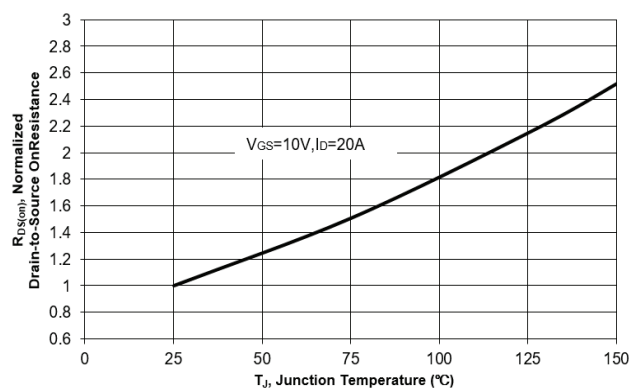
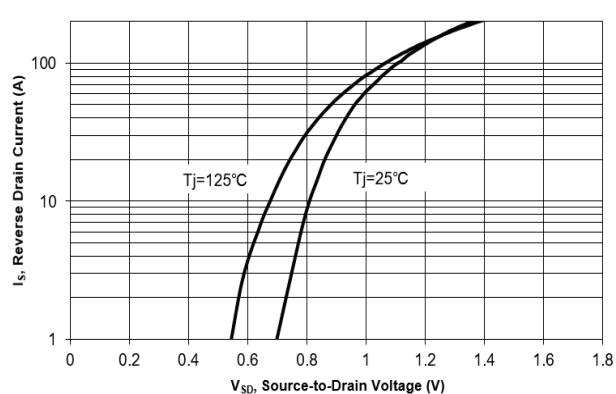


Fig. 6 Typical Body-Diode Forward Characteristics



Electrical Characteristics Curves

Fig. 13 Normalized Maximum Transient Thermal Impedance($Z_{\theta JC}$)

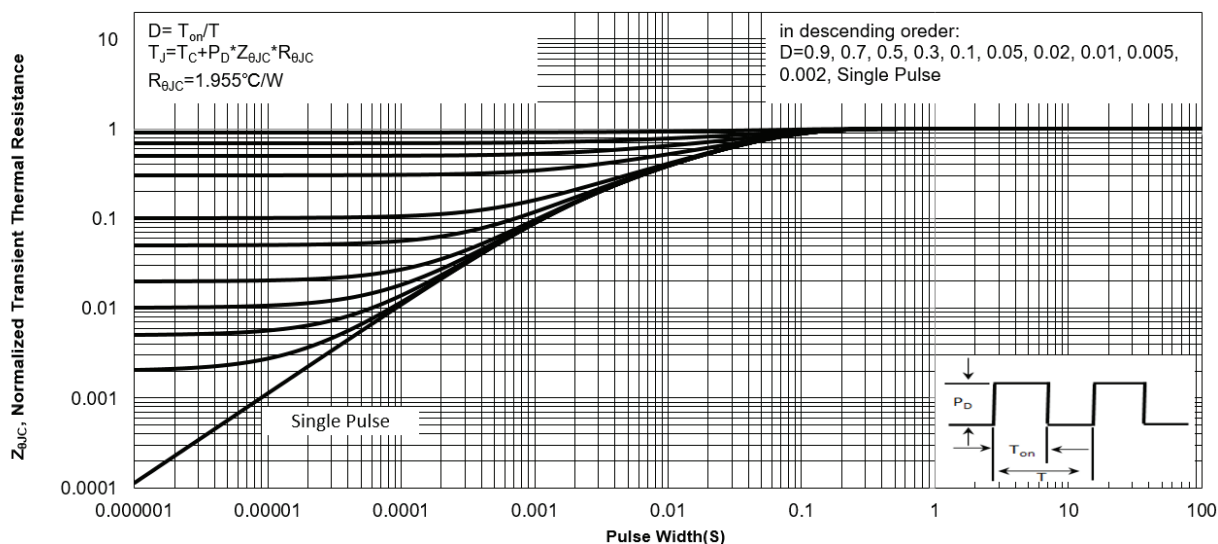


Fig. 14 Normalized Maximum Transient Thermal Impedance($Z_{\theta JA}$)

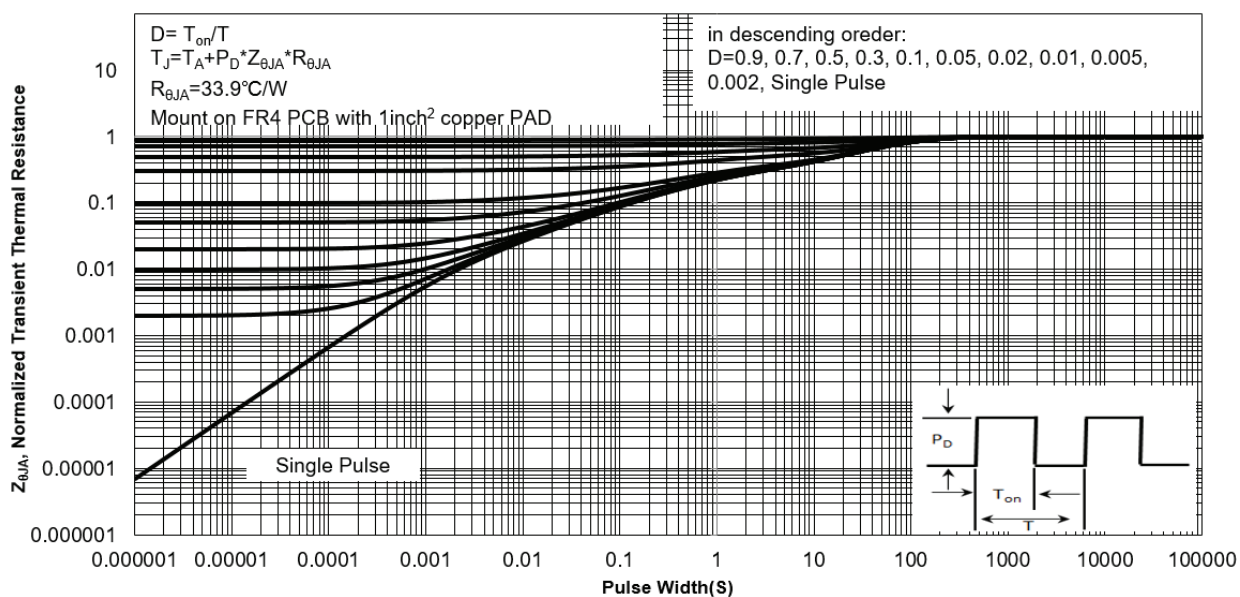


Fig. 7 Typical Junction Capacitance

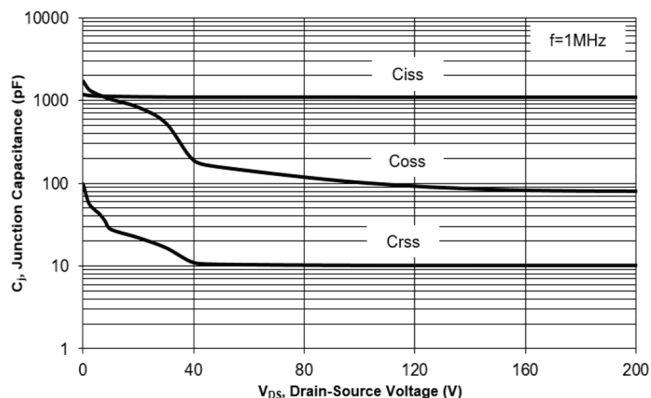


Fig. 8 Drain-Source Leakage Current vs. T_J

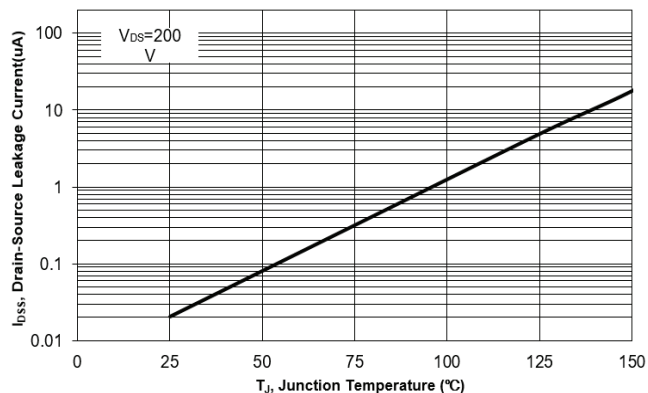


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

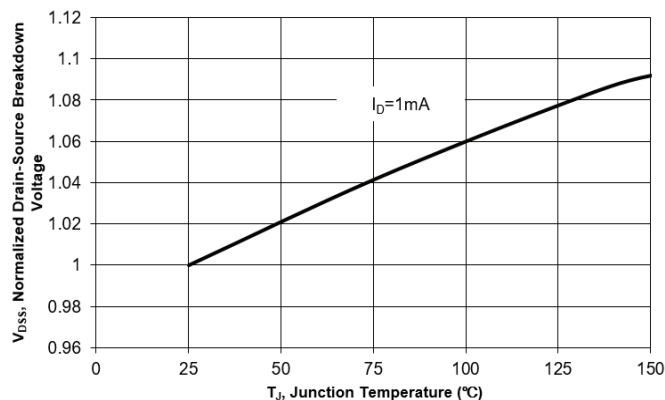


Fig. 10 Gate Threshold Variation vs. T_J

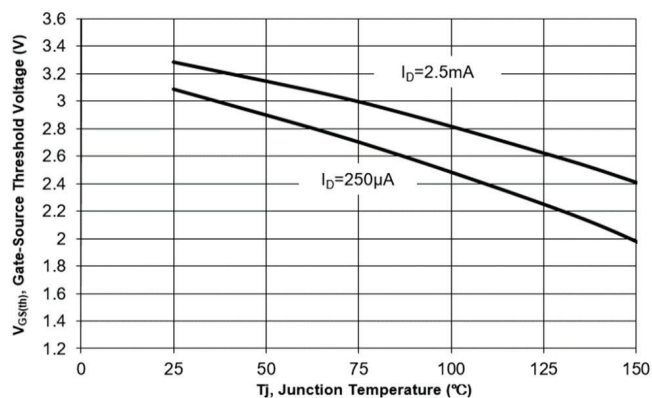


Fig. 11 Gate Charge

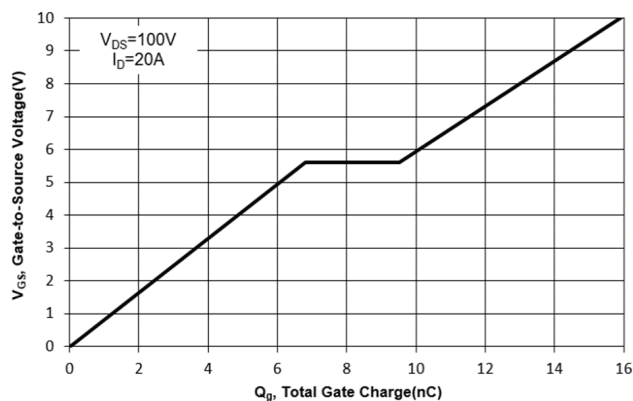
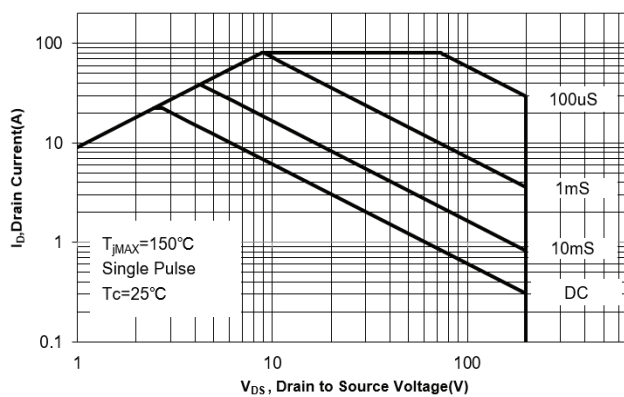


Fig. 12 Safe Operation Area



Test Circuits

Fig.1-1 Switching times test circuit

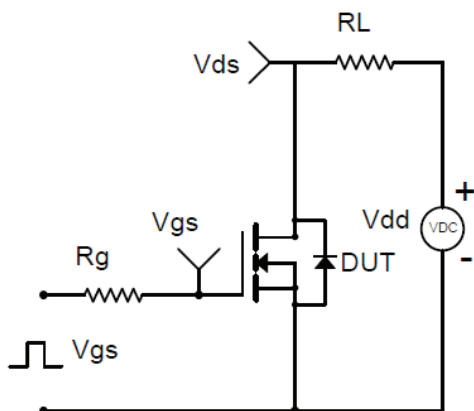


Fig.1-2 Switching Waveform

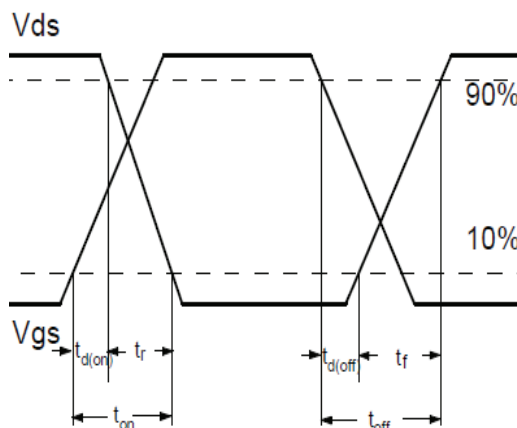


Fig.2-1 Gate charge test circuit

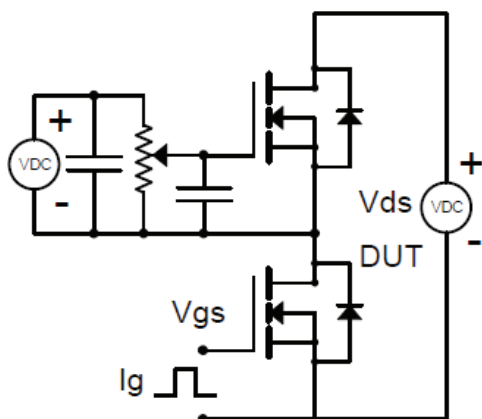


Fig.2-2 Gate charge waveform

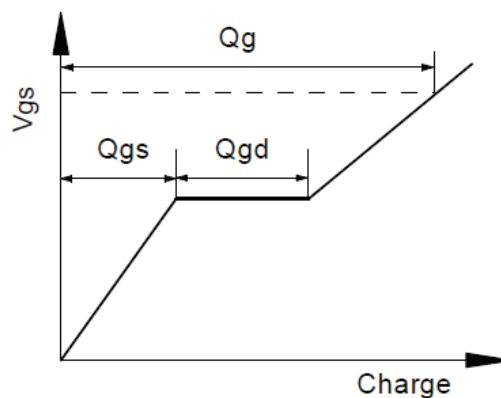


Fig.3-1 Avalanche test circuit

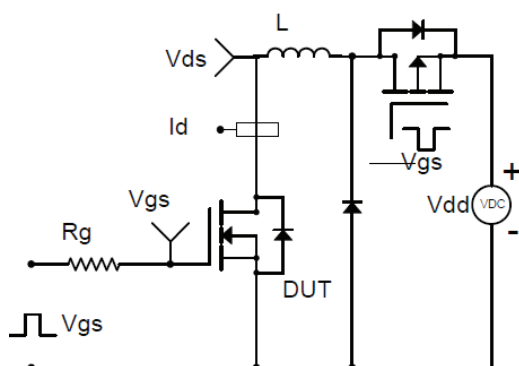
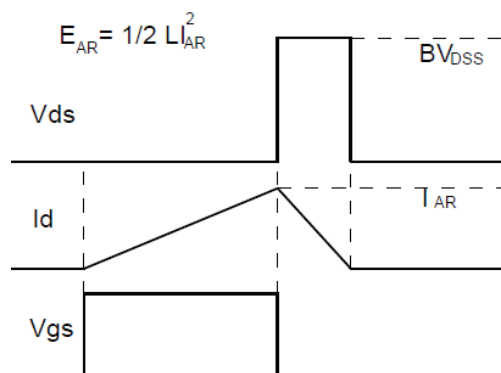
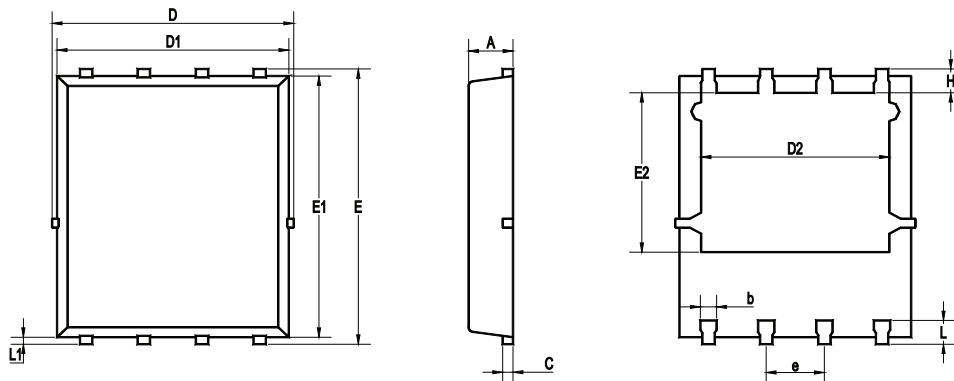


Fig.3-2 Avalanche waveform



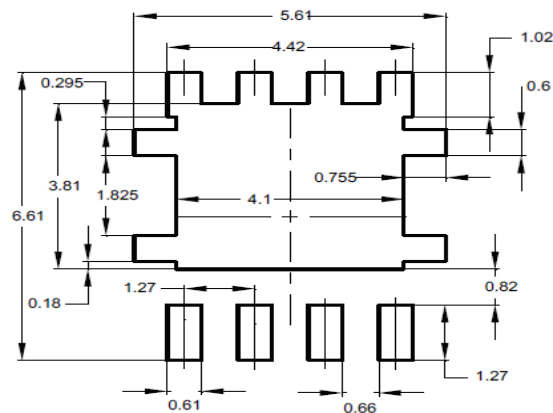
Package Outline Dimensions (Units: mm)

DFN5060



UNIT	A	b	C	D	D1	D2	E	E1	E2	e	L	L1	H
mm	1.12 0.9	0.51 0.33	0.34 0.11	5.26 4.7	5.1 4.7	4.5 3.56	6.25 5.75	6 5.6	3.66 3.18	1.37 1.17	0.71 0.35	0.2 0.06	0.71 0.35

Recommended Soldering Footprint



Packing information

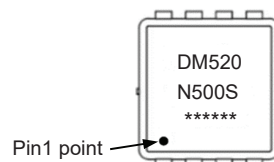
Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
DFN5060	12	8 ± 0.1	0.315 ± 0.004	330	13	5,000

Marking information

" DM520N500S " = Part No.

" ***** " = Date Code Marking

Font type: Arial



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