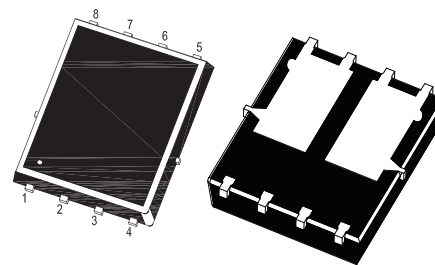
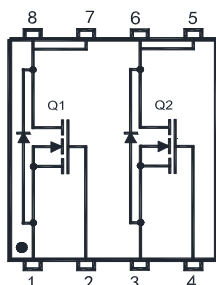


Dual N-Channel Enhancement Mode MOSFET

Features

- Low $R_{DS(ON)}$
- AEC-Q101 Qualified
- Surface-mounted package
- Halogen and Antimony Free(HAF), RoHS compliant



Q1:1.Source 2.Gate 7.Drain 8.Drain
 Q2:3.Source 4.Gate 5.Drain 6.Drain
 DFN5060 Plastic Package

Application

- DC-DC Power supply

Key Parameters(Q1/Q2)

Parameter	Value	Unit
BV_{DSS}	40	V
$R_{DS(ON)}$ Max	34 @ $V_{GS} = 10\text{ V}$	m Ω
	45 @ $V_{GS} = 4.5\text{ V}$	
$V_{GS(th)}$ typ	1.6	V
Q_g typ	9.4 @ $V_{GS} = 10\text{ V}$	nC

Absolute Maximum Ratings(at $T_a = 25^\circ\text{C}$ unless otherwise specified)(Q1/Q2)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	14	A
		8.8	
Peak Drain Current, Pulsed ¹⁾	I_{DM}	36	A
Avalanche Current	I_{AS}	10	A
Single Pulse Avalanche Energy ²⁾	E_{AS}	5	mJ
Power Dissipation	P_D	11.9	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$

Thermal Characteristics(Q1/Q2)

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	10.5	$^\circ\text{C/W}$
Thermal Resistance from Junction to Ambient ³⁾	$R_{\theta JA}$	65	$^\circ\text{C/W}$

¹⁾ Pulse Test: Pulse Width $\leq 100\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.

²⁾ Limited by $T_{J(MAX)}$, starting $T_J = 25^\circ\text{C}$, $L = 0.1\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 10\text{ A}$, $V_{GS} = 10\text{ V}$.

³⁾ Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

Characteristics at T_a = 25°C unless otherwise specified(Q1/Q2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I _D = 250 μ A	BV _{DSS}	40	-	-	V
Drain-Source Leakage Current at V _{DS} = 32 V	I _{DSS}	-	-	1	μ A
Gate Leakage Current at V _{GS} = $\pm$ 16 V	I _{GSS}	-	-	$\pm$ 100	nA
Gate-Source Threshold Voltage at V _{DS} = V _{GS} , I _D = 250 μ A	V _{GS(th)}	1	-	2.5	V
Drain-Source On-State Resistance at V _{GS} = 10 V, I _D = 5 A at V _{GS} = 4.5 V, I _D = 3 A	R _{DS(on)}	- -	27 -	34 45	m Ω
DYNAMIC PARAMETERS					
Forward Transconductance at V _{DS} = 5 V, I _D = 5 A	g _{fs}	-	7	-	S
Gate resistance at V _{DS} = 0 V, V _{GS} = 0 V, f = 1 MHz	R _g	-	1.2	-	Ω
Input Capacitance at V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz	C _{iss}	-	415	-	pF
Output Capacitance at V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz	C _{oss}	-	38	-	pF
Reverse Transfer Capacitance at V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz	C _{rss}	-	33	-	pF
Gate charge total at V _{DS} = 20 V, I _D = 5 A, V _{GS} = 10 V at V _{DS} = 20 V, I _D = 5 A, V _{GS} = 4.5 V	Q _g	- -	9.4 4.4	- -	nC
Gate to Source Charge at V _{DS} = 20 V, I _D = 5 A, V _{GS} = 10 V	Q _{gs}	-	1.8	-	nC
Gate to Drain Charge at V _{DS} = 20 V, I _D = 5 A, V _{GS} = 10 V	Q _{gd}	-	1.7	-	nC
Turn-On Delay Time at V _{DS} = 20 V, I _D = 5 A, V _{GS} = 10 V, R _g = 1 Ω	t _{d(on)}	-	6	-	ns
Turn-On Rise Time at V _{DS} = 20 V, I _D = 5 A, V _{GS} = 10 V, R _g = 1 Ω	t _r	-	8	-	ns
Turn-Off Delay Time at V _{DS} = 20 V, I _D = 5 A, V _{GS} = 10 V, R _g = 1 Ω	t _{d(off)}	-	6	-	ns
Turn-Off Fall Time at V _{DS} = 20 V, I _D = 5 A, V _{GS} = 10 V, R _g = 1 Ω	t _f	-	1.3	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I _S = 5 A, V _{GS} = 0 V	V _{SD}	-	-	1.2	V
Body-Diode Continuous Current	I _S	-	-	14	A
Body-Diode Continuous Current, Pulsed	I _{SM}	-	-	36	A
Body Diode Reverse Recovery Time at I _S = 5 A, di/dt = 100 A / μ s	t _{rr}	-	6.2	-	ns
Body Diode Reverse Recovery Charge at I _S = 5 A, di/dt = 100 A / μ s	Q _{rr}	-	2.6	-	nC

Electrical Characteristics Curves(Q1/Q2)

Fig. 1 Typical Output Characteristics

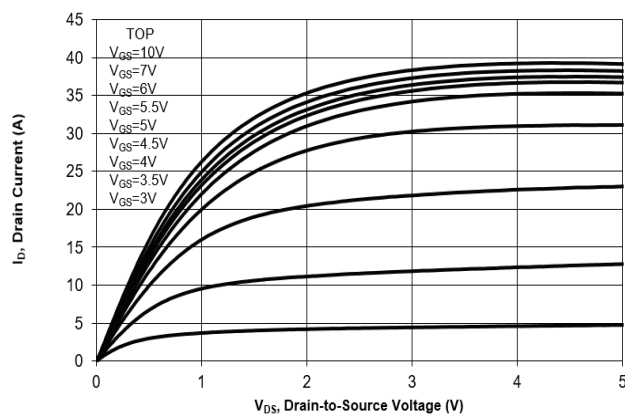


Fig. 2 Typical Transfer Characteristics

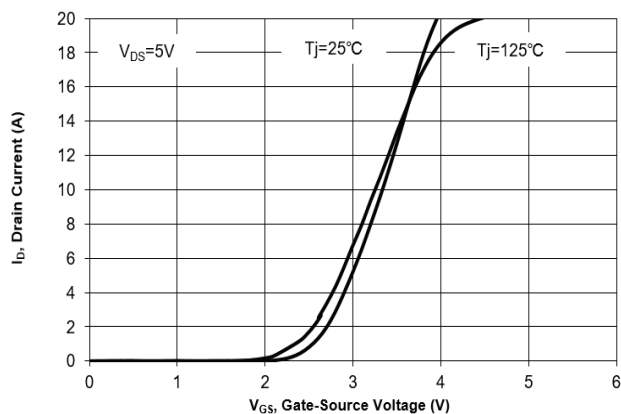


Fig. 3 on-Resistance vs Drain Current

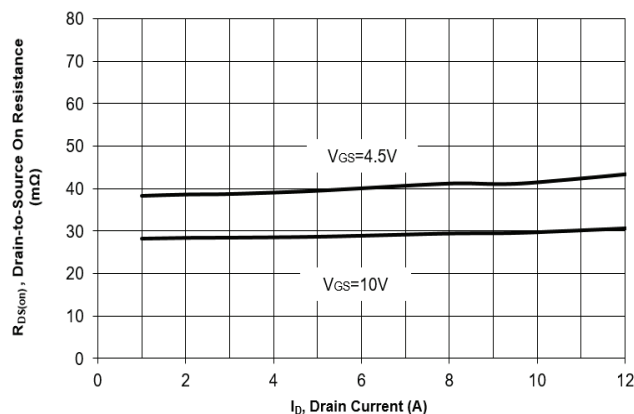


Fig. 4 on-Resistance vs. Gate to Source Voltage

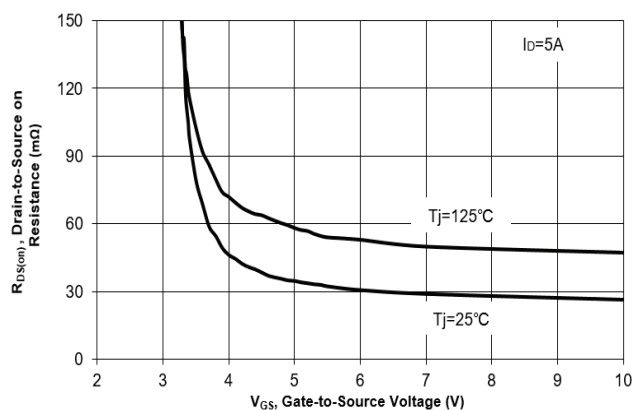


Fig. 5 on-Resistance vs. T_J

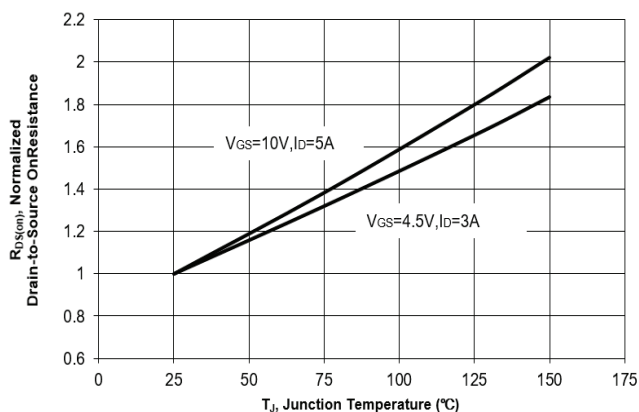
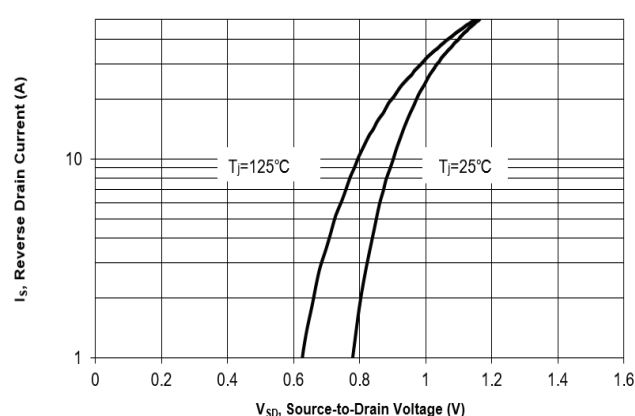


Fig. 6 Typical Body Diode Forward Characteristics



Electrical Characteristics Curves(Q1/Q2)

Fig. 7 Typical Junction Capacitance

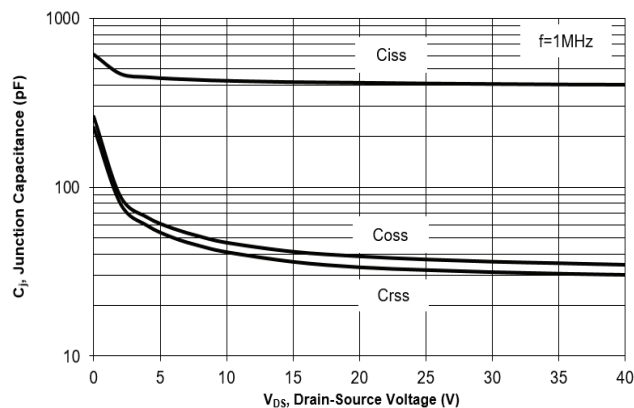


Fig. 8 Drain-Source Leakage Current vs. T_j

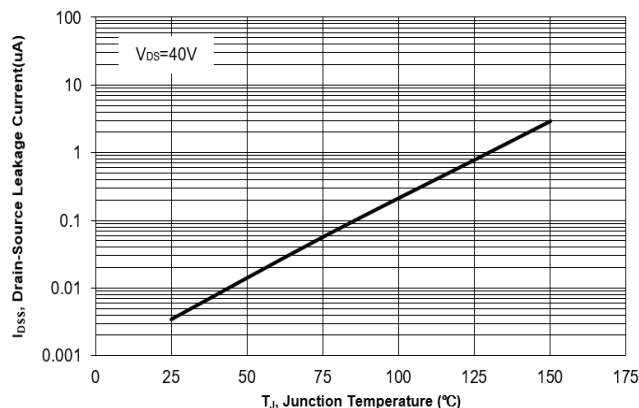


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

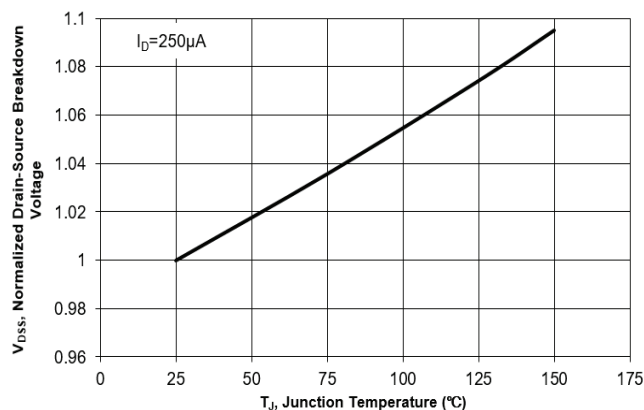


Fig. 10 Gate Threshold Variation vs. T_j

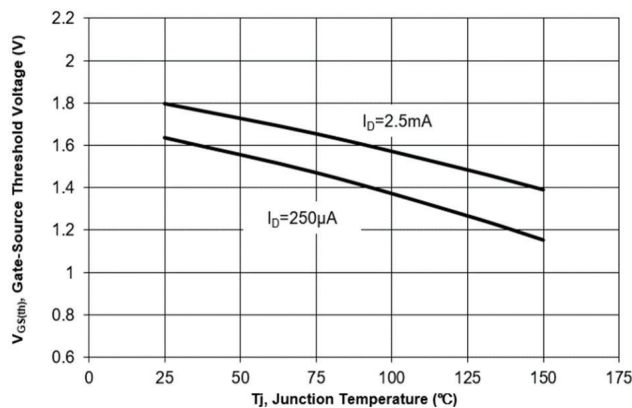


Fig. 11 Gate Charge

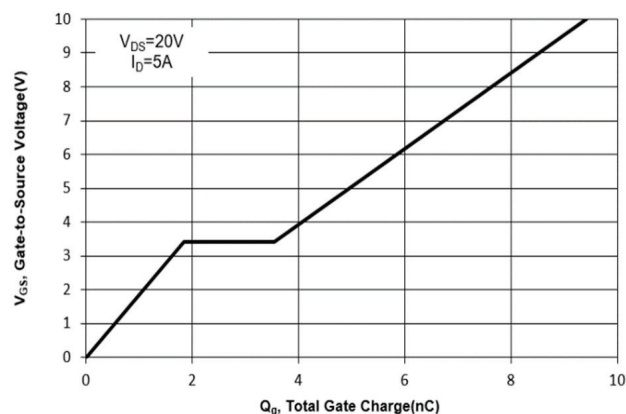
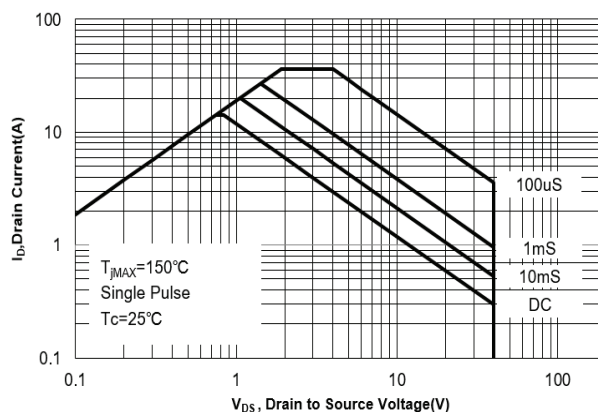
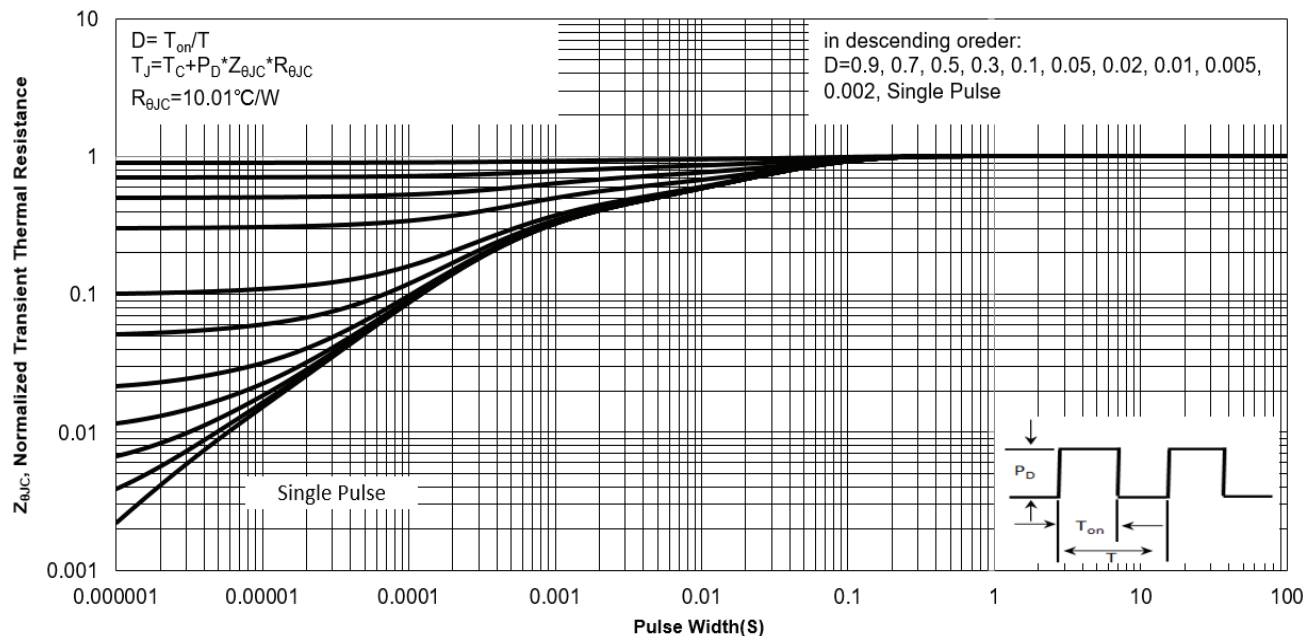
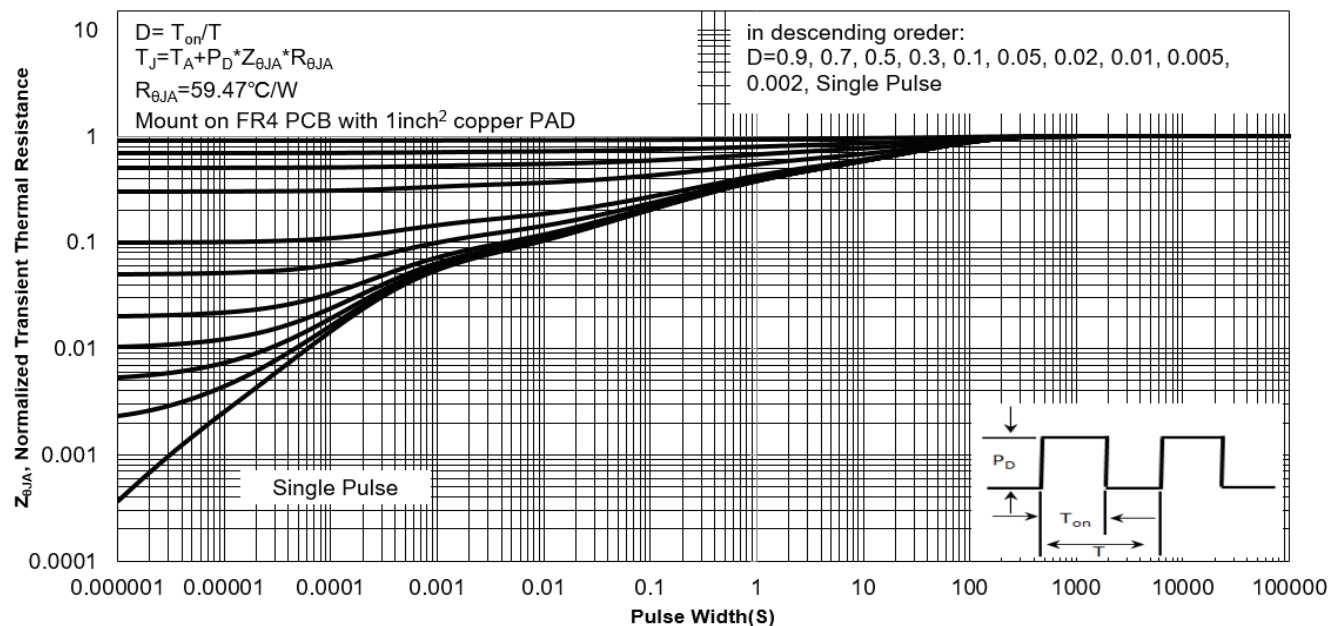


Fig. 12 Safe Operation Area



Electrical Characteristics Curves(Q1/Q2)
Fig.13 Normalized Maximum Transient Thermal Impedance($z_{\theta JC}$)

Fig.14 Normalized Maximum Transient Thermal Impedance($z_{\theta JA}$)


Test Circuits(Q1/Q2)

Fig.1-1 Switching times test circuit

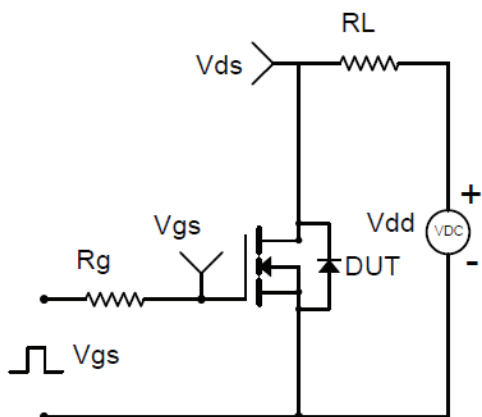


Fig.1-2 Switching Waveform

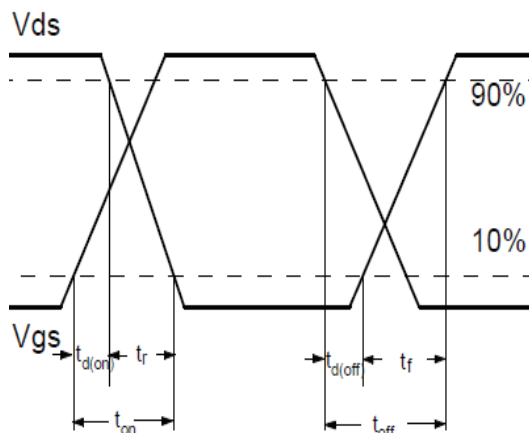


Fig.2-1 Gate charge test circuit

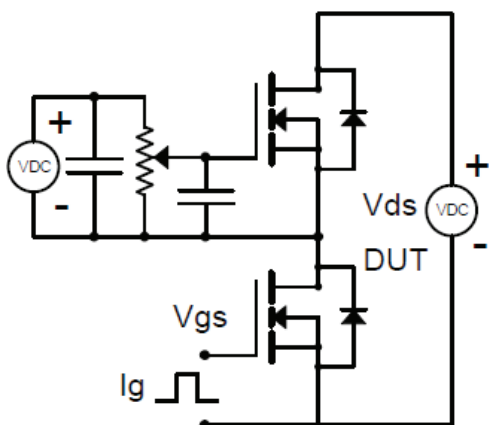


Fig.2-2 Gate charge waveform

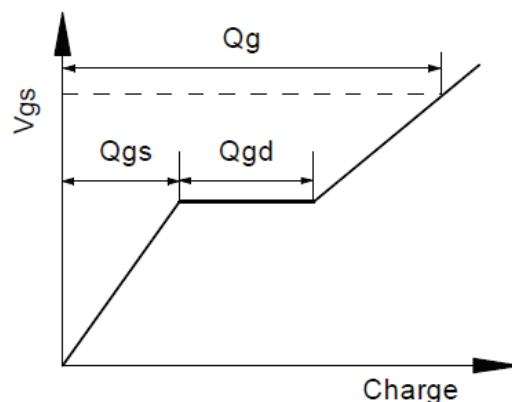


Fig.3-1 Avalanche test circuit

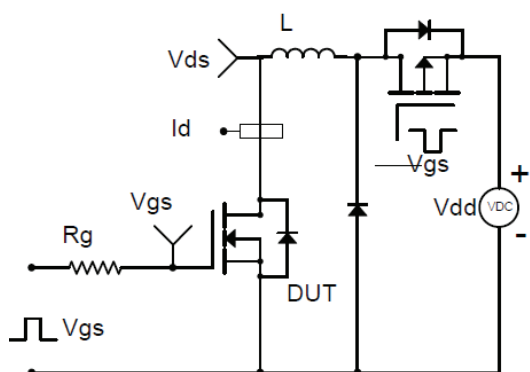
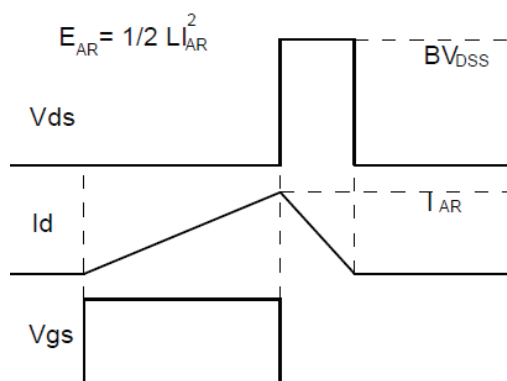
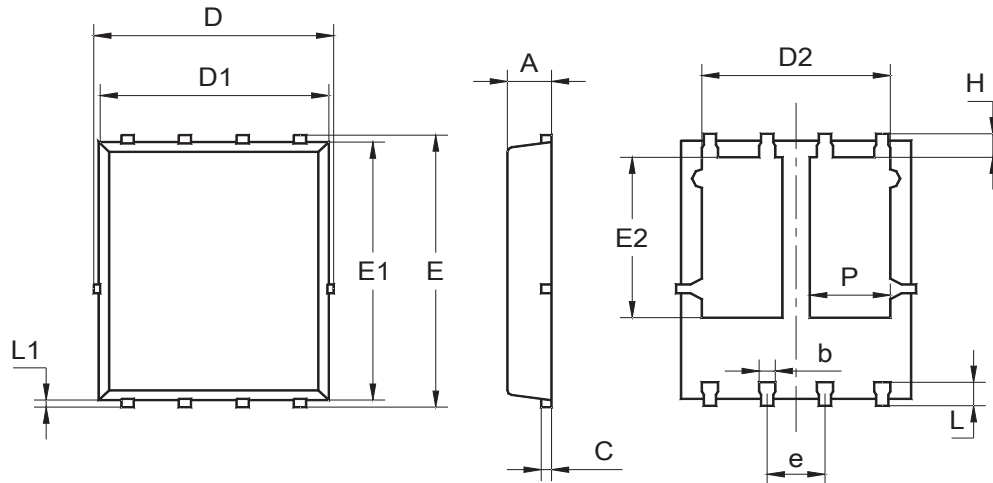
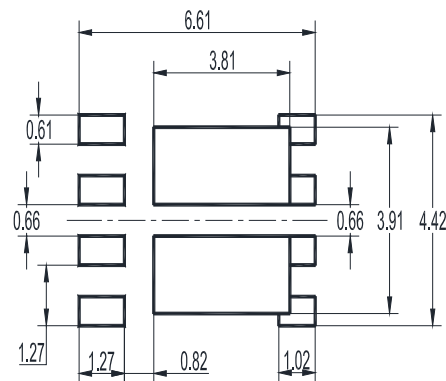


Fig.3-2 Avalanche waveform



Package Outline Dimensions (Units: mm)
DFN5060


Unit	A	b	C	D	D1	D2	E	E1	E2	e	L	L1	H	P
mm	1.12 0.9	0.51 0.33	0.34 0.11	5.26 4.7	5.1 4.7	4.5 3.56	6.25 5.75	6 5.6	3.66 3.18	1.37 1.17	0.71 0.35	0.2 0.06	0.71 0.35	2.3 1.7

Recommended Soldering Footprint

Packing information

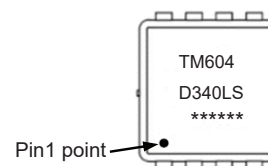
Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
DFN5060	12	8 ± 0.1	0.315 ± 0.004	330	13	5,000

Marking information

" TM604D340LS " = Part No.

" ***** " = Date Code Marking

Font type: Arial



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