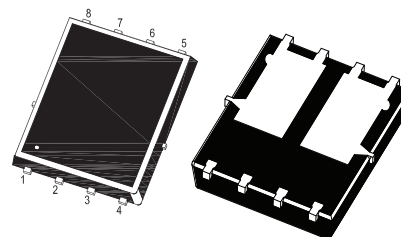
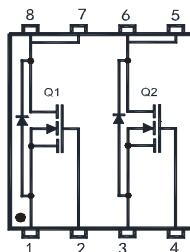


Dual N-Channel Enhancement Mode MOSFET

Features

- Low $R_{DS(ON)}$
- AEC-Q101 Qualified
- Fully Characterized Capacitance and Avalanche
- Halogen and Antimony Free(HAF), RoHS compliant



Q1:1.Source 2.Gate 7.Drain 8.Drain
Q2:3.Source 4.Gate 5.Drain 6.Drain
DFN5060 Plastic Package

Application

- Synchronous Rectification
- BLDC Motor drive applications
- Battery powered circuits

Key Parameters(Q1/Q2)

Parameter	Value	Unit
BV_{DSS}	100	V
$R_{DS(ON)}$ Max	18 @ $V_{GS} = 10$ V	m Ω
	24 @ $V_{GS} = 4.5$ V	
$V_{GS(th)}$ typ	1.9	V
Q_g typ	22 @ $V_{GS} = 10$ V	nC

Absolute Maximum Ratings (at $T_a = 25^\circ\text{C}$ unless otherwise specified)(Q1\Q2)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	34	A
		21	
Peak Drain Current, Pulsed ¹⁾	I_{DM}	130	A
Avalanche Current	I_{AS}	17.4	A
Single Pulse Avalanche Energy ²⁾	E_{AS}	15	mJ
Power Dissipation	P_{tot}	79	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	$^\circ\text{C}$

Thermal Characteristics(Q1\Q2)

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case $t \leq 10$ ms	$R_{\theta JC}$	1.9	$^\circ\text{C/W}$
Thermal Resistance from Junction to Case	$R_{\theta JC}$	3.8	$^\circ\text{C/W}$
Thermal Resistance from Junction to Ambient ³⁾	$R_{\theta JA}$	80	$^\circ\text{C/W}$

¹⁾ Pulse Test: Pulse Width ≤ 100 μs , Duty Cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 175^\circ\text{C}$.

²⁾ Limited by $T_{J(MAX)}$, starting $T_J = 25^\circ\text{C}$, $L = 0.1$ mH, $R_g = 25$ Ω , $I_{AS} = 17.4$ A, $V_{GS} = 10$ V.

³⁾ Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

Characteristics at T_a = 25°C unless otherwise specified(Q1/Q2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I _D = 250 μA	BV _{DSS}	100	-	-	V
Drain-Source Leakage Current at V _{DS} = 80 V	I _{DSS}	-	-	1	μA
Gate Leakage Current at V _{GS} = ± 20 V	I _{GSS}	-	-	± 100	nA
Gate-Source Threshold Voltage at V _{DS} = V _{GS} , I _D = 250 μA	V _{GS(th)}	1.2	-	2.5	V
Drain-Source On-State Resistance at V _{GS} = 10 V, I _D = 7 A at V _{GS} = 4.5 V, I _D = 5 A	R _{DS(on)}	- -	15 -	18 24	mΩ
DYNAMIC PARAMETERS					
Forward Transconductance at V _{DS} = 5 V, I _D = 7 A	g _{fs}	-	15.8	-	S
Gate resistance at V _{GS} = 0 V, V _{DS} = 0 V, f = 1 MHz	R _g	-	0.6	-	Ω
Input Capacitance at V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	C _{iss}	-	1054	-	pF
Output Capacitance at V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	C _{oss}	-	446	-	pF
Reverse Transfer Capacitance at V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	C _{rss}	-	36	-	pF
Gate charge total at V _{DS} = 50 V, V _{GS} = 10 V, I _D = 20 A at V _{DS} = 50 V, V _{GS} = 4.5 V, I _D = 20 A	Q _g	- -	22 11.5	- -	nC
Gate to Source Charge at V _{DS} = 50 V, V _{GS} = 10 V, I _D = 20 A	Q _{gs}	-	4.6	-	nC
Gate to Drain Charge at V _{DS} = 50 V, V _{GS} = 10 V, I _D = 20 A	Q _{gd}	-	6.3	-	nC
Turn-On Delay Time at V _{DS} = 50 V, V _{GS} = 10 V, I _D = 20 A, R _g = 3 Ω	t _{d(on)}	-	11	-	ns
Turn-On Rise Time at V _{DS} = 50 V, V _{GS} = 10 V, I _D = 20 A, R _g = 3 Ω	t _r	-	17	-	ns
Turn-Off Delay Time at V _{DS} = 50 V, V _{GS} = 10 V, I _D = 20 A, R _g = 3 Ω	t _{d(off)}	-	10	-	ns
Turn-Off Fall Time at V _{DS} = 50 V, V _{GS} = 10 V, I _D = 20 A, R _g = 3 Ω	t _f	-	2	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I _S = 1 A, V _{GS} = 0 V	V _{SD}	-	-	1.2	V
Body-Diode Continuous Current	I _S	-	-	34	A
Body-Diode Continuous Current, Pulsed	I _{SM}	-	-	130	A
Body Diode Reverse Recovery Time at I _S = 7 A, di/dt = 100 A / μs	t _{rr}	-	40	-	ns
Body Diode Reverse Recovery Charge at I _S = 7 A, di/dt = 100 A / μs	Q _{rr}	-	30	-	nC

Electrical Characteristics Curves(Q1/Q2)

Fig. 1 Typical Output Characteristics

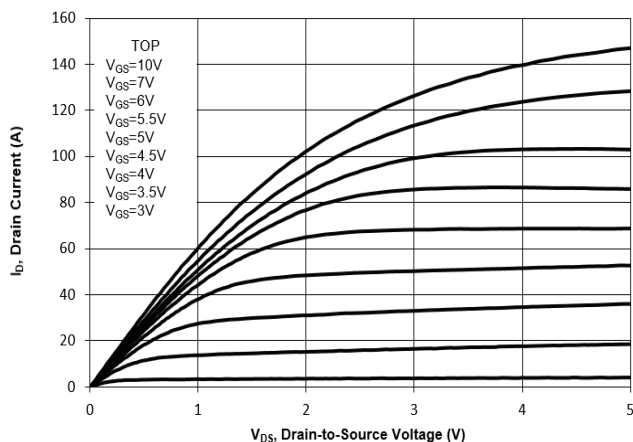


Fig. 2 Typical Transfer Characteristics

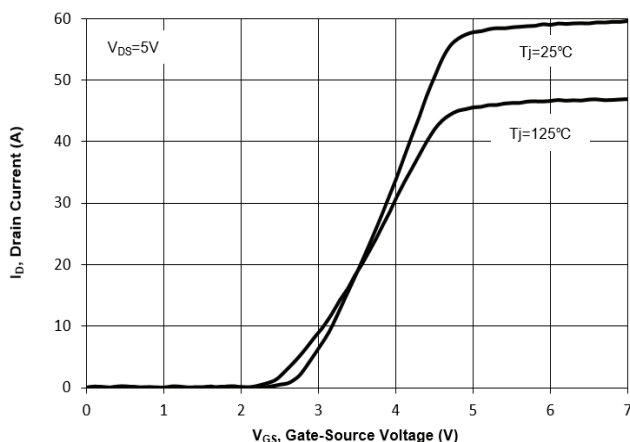


Fig. 3 On-Resistance vs. Drain Current

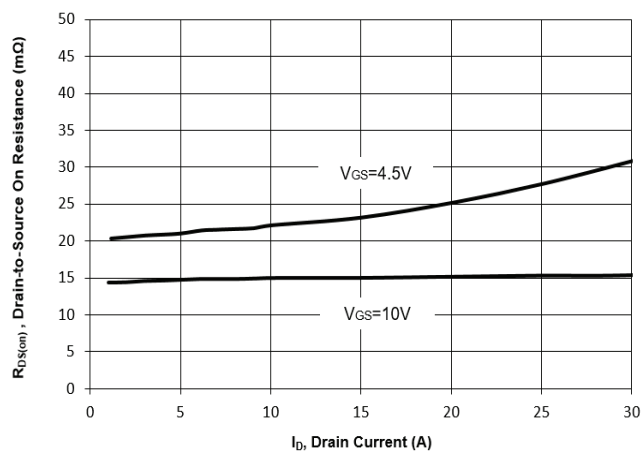


Fig. 4 On-Resistance vs. Gate to Source Voltage

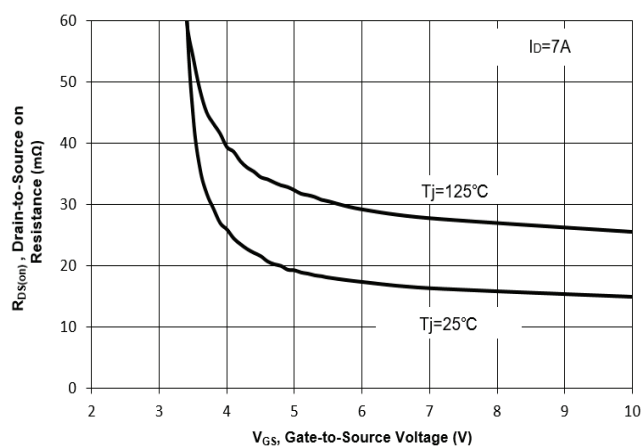


Fig. 5 On-Resistance vs. T_J

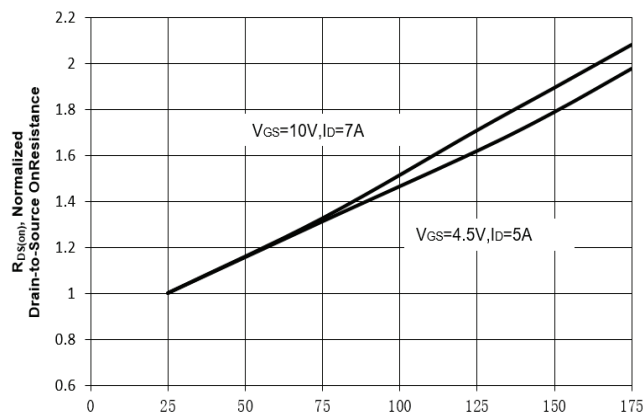
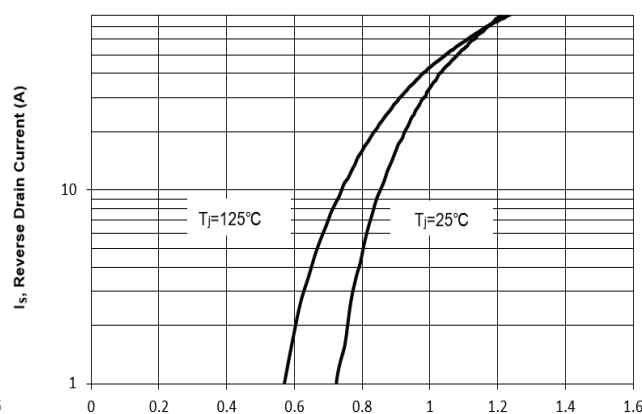


Fig. 6 Typical Body-Diode Forward Characteristics



Electrical Characteristics Curves(Q1/Q2)

Fig. 13 Normalized Maximum Transient Thermal Impedance($Z_{\theta JC}$)

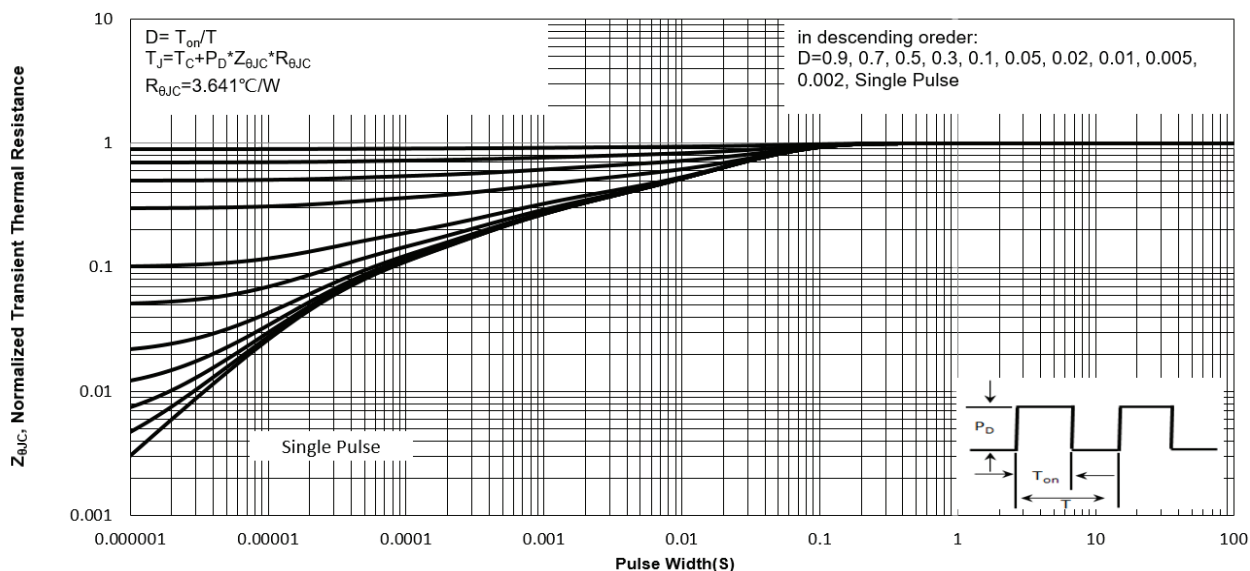


Fig. 14 Normalized Maximum Transient Thermal Impedance($Z_{\theta JA}$)

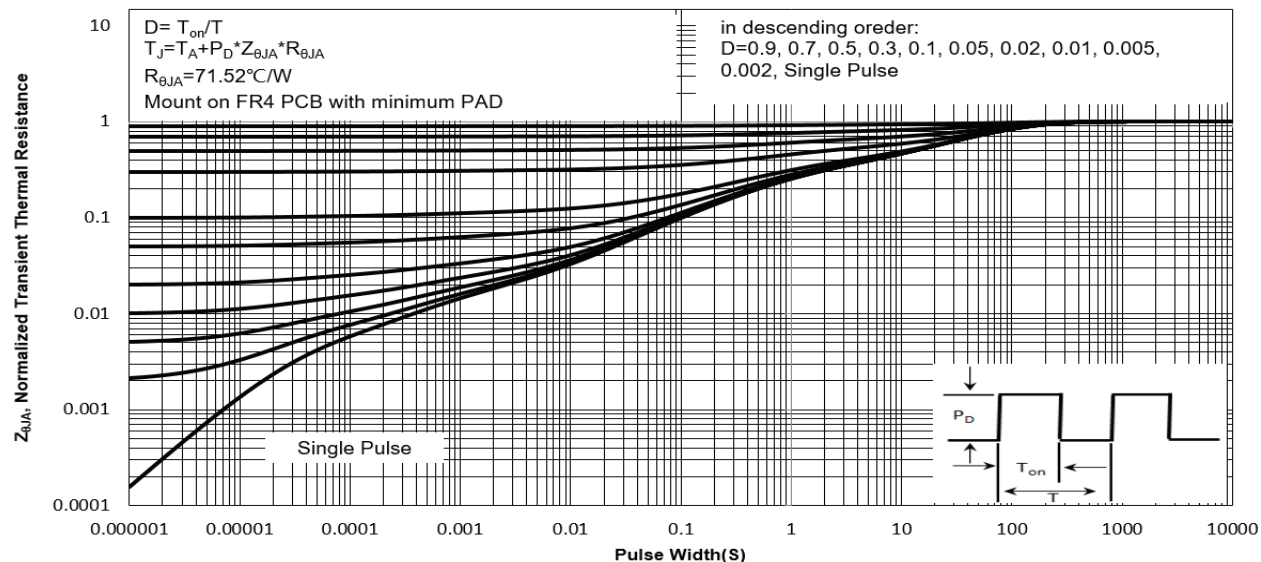


Fig. 7 Typical Junction Capacitance

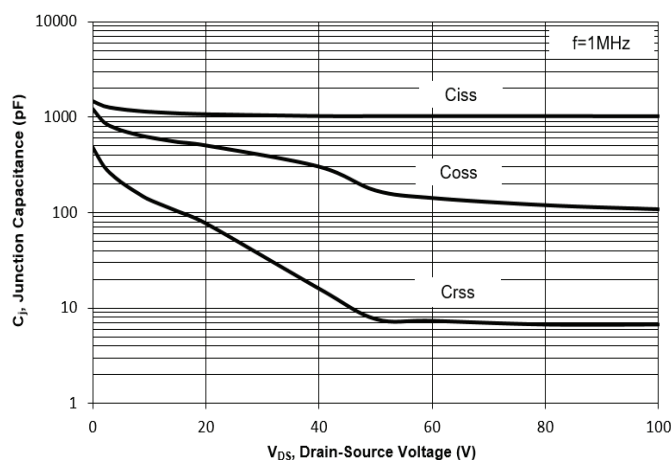


Fig. 8 Drain-Source Leakage Current vs. T_j

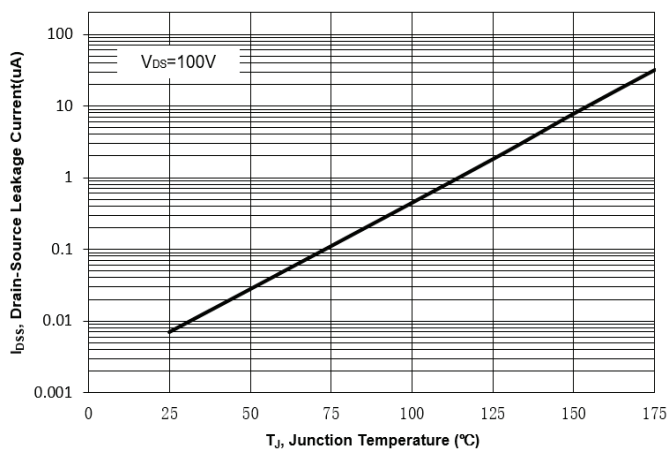


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

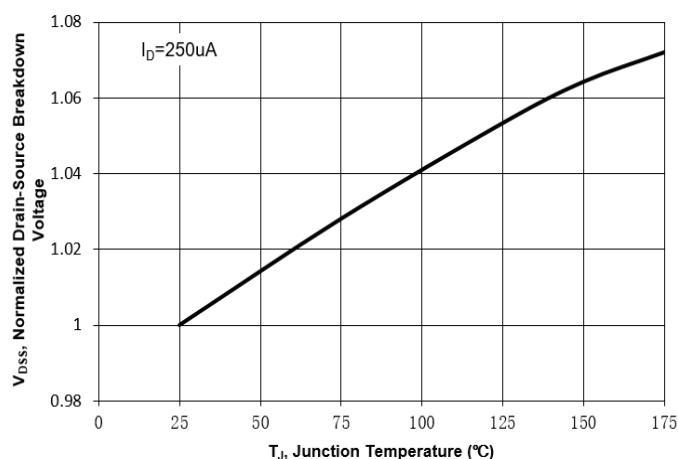


Fig. 10 Gate Threshold Variation vs. T_j

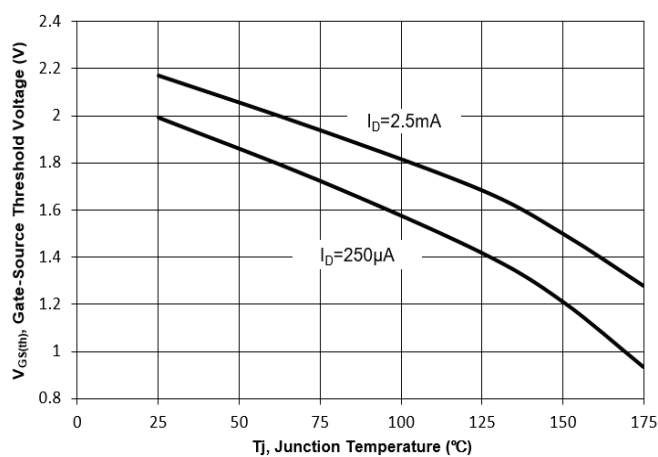


Fig. 11 Gate Charge

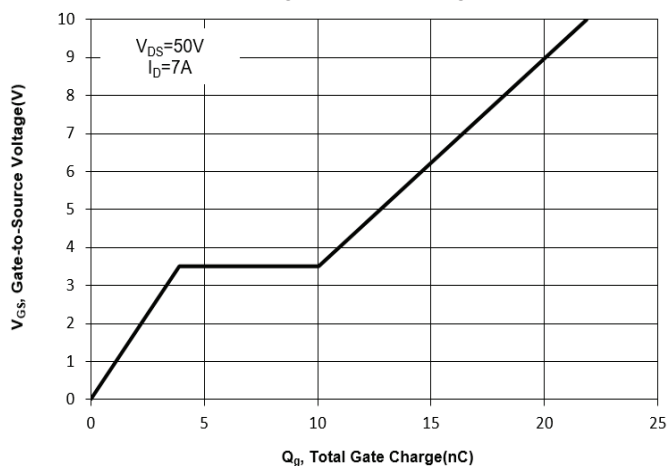
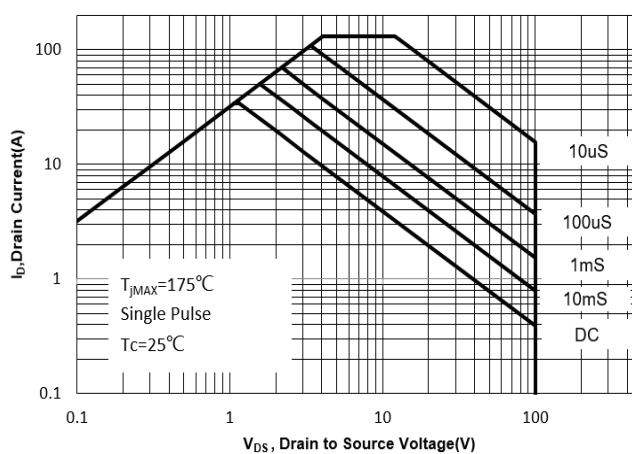
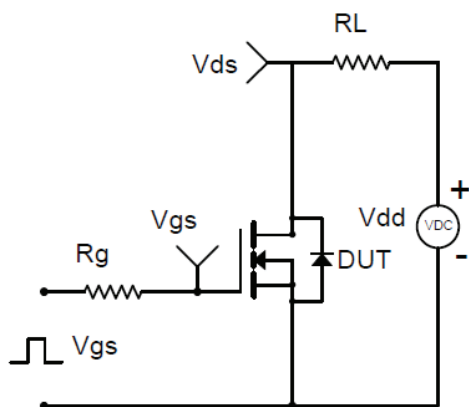
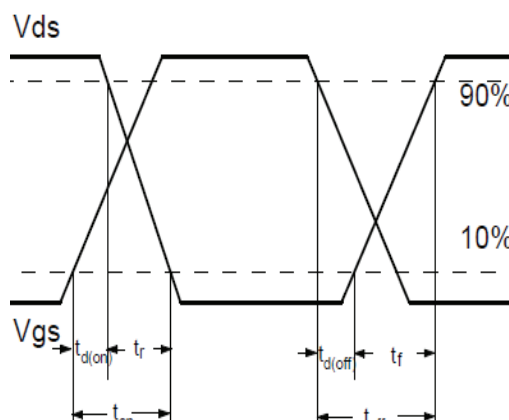
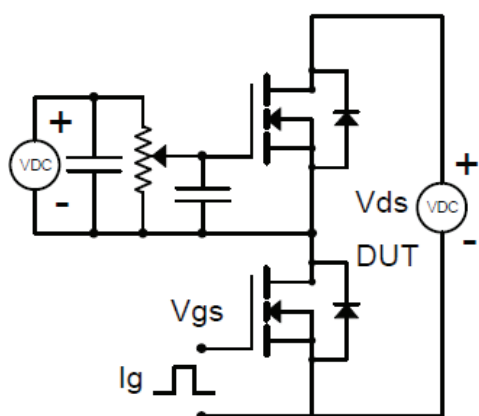
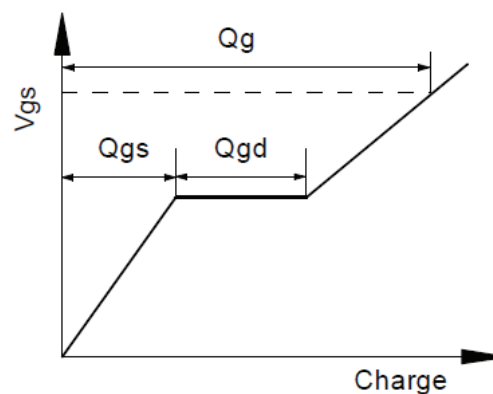
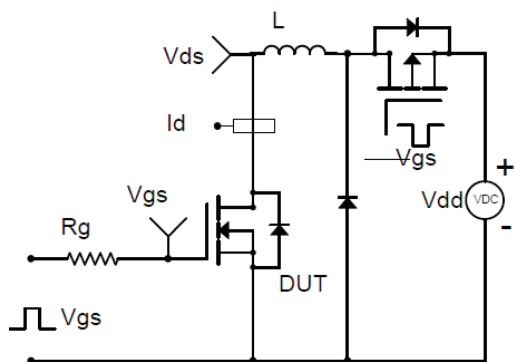
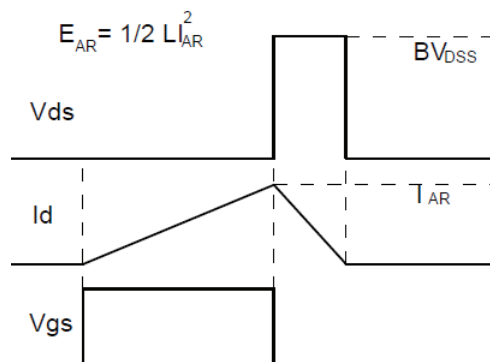


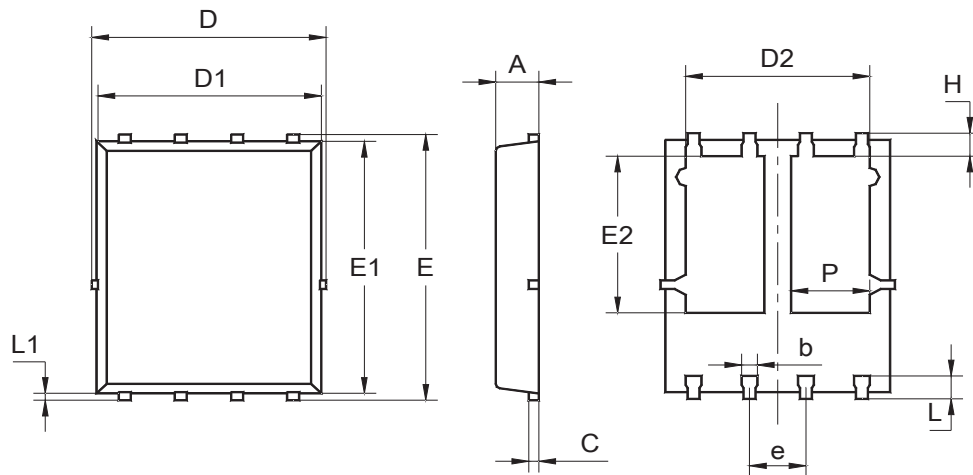
Fig. 12 Safe Operation Area



Test Circuits(Q1/Q2)
Fig.1-1 Switching times test circuit

Fig.1-2 Switching Waveform

Fig.2-1 Gate charge test circuit

Fig.2-2 Gate charge waveform

Fig.3-1 Avalanche test circuit

Fig.3-2 Avalanche waveform


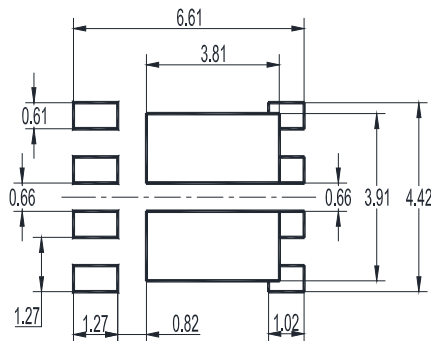
Package Outline Dimensions (Units: mm)

DFN5060



Unit	A	b	C	D	D1	D2	E	E1	E2	e	L	L1	H	P
mm	1.12	0.51	0.34	5.26	5.1	4.5	6.25	6	3.66	1.37	0.71	0.2	0.71	2.3
	0.9	0.33	0.11	4.7	4.7	3.56	5.75	5.6	3.18	1.17	0.35	0.06	0.35	1.7

Recommended Soldering Footprint



Packing information

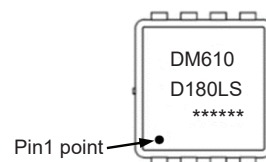
Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
DFN5060	12	8 ± 0.1	0.315 ± 0.004	330	13	5,000

Marking information

" DM610D180LS " = Part No.

" ***** " = Date Code Marking

Font type: Arial



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