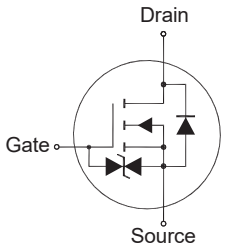
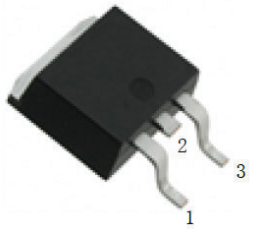
N-Channel Enhancement Mode MOSFET





1.Gate 2.Drain 3.Source

TO-252 Plastic Package

Features

- AEC-Q101 Qualified
- Surface-mounted package
- Built-in G-S Protection Diode
- Halogen and Antimony Free(HAF), RoHS compliant
- Typical ESD Protection HBM Class 2

Classification	Voltage Range(V)
0A	< 125
0B	125 to < 250
1A	250 to < 500
1B	500 to < 1000
1C	1000 to < 2000
2	2000 to < 4000
3A	4000 to < 8000
3B	≥ 8000

Key Parameters

Parameter	Value	Unit
BV_{DSS}	100	V
$R_{DS(ON)}$ Max	68 @ V_{GS} = 10 V	mΩ
	92 @ V_{GS} = 4.5 V	
$V_{GS(th)}$ typ	1.9	V
Q_g typ	9 @ V_{GS} = 10 V	nC

Absolute Maximum Ratings(at T_a = 25℃ unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current	T_c = 25℃ T_c = 100℃	I_D	17.8 12.4	A
Peak Drain Current, Pulsed [1]		I_{DM}	45	A
Avalanche Current		I_{AS}	4.9	A
Single Pulse Avalanche Energy [2]		E_{AS}	6	mJ
Power Dissipation	T_c = 25℃	P_{tot}	34.8	W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	℃

Thermal Characteristics

Parameter	Symbol	Max.	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	4.3	℃/W
Thermal Resistance from Junction to Ambient [3]	$R_{\theta JA}$	37	℃/W

[1] Pulse Test: Pulse Width ≤ 100 μs, Duty Cycle ≤ 2%, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$ = 175°C.

[2] Limited by $T_{J(MAX)}$, starting T_J = 25 °C, L = 0.5 mH, R_g = 25 Ω, I_{AS} = 4.9 A, V_{GS} = 10 V.

[3] Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.

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Characteristics at T_a = 25℃ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit
STATIC PARAMETERS					
Drain-Source Breakdown Voltage at I_D = 250 µA	BV_{DSS}	100	-	-	V
Drain-Source Leakage Current at V_{DS} = 80 V	I_{DSS}	-	-	1	µA
Gate Leakage Current at V_{GS} = ± 16 V	I_{GSS}	-	-	± 10	µA
Gate-Source Threshold Voltage at V_{DS} = V_{GS}, I_D = 250 µA	$V_{GS(th)}$	1.7	-	2.5	V
Drain-Source On-State Resistance at V_{GS} = 10 V, I_D = 10 A at V_{GS} = 4.5 V, I_D = 8 A	$R_{DS(on)}$	- -	53 -	68 92	mΩ
DYNAMIC PARAMETERS					
Forward Transconductance at V_{DS} = 5 V, I_D = 8 A	g_{fs}	-	9.9	-	S
Gate Resistance at V_{GS} = 0 V, V_{DS} = 0 V, f = 1 MHz	R_g	-	0.7	-	Ω
Input Capacitance at V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	C_{iss}	-	317	-	pF
Output Capacitance at V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	C_{oss}	-	61	-	pF
Reverse Transfer Capacitance at V_{GS} = 0 V, V_{DS} = 50 V, f = 1 MHz	C_{rss}	-	7	-	pF
Gate charge total at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 10 A at V_{DS} = 50 V, V_{GS} = 4.5 V, I_D = 10 A	Q_g	- -	9 4.7	- -	nC
Gate to Source Charge at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 10 A	Q_{gs}	-	1.7	-	nC
Gate to Drain Charge at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 10 A	Q_{gd}	-	3	-	nC
Turn-On Delay Time at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 10 A, R_g = 3.3 Ω	$t_{d(on)}$	-	6	-	ns
Turn-On Rise Time at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 10 A, R_g = 3.3 Ω	t_r	-	8	-	ns
Turn-Off Delay Time at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 10 A, R_g = 3.3 Ω	$t_{d(off)}$	-	6	-	ns
Turn-Off Fall Time at V_{DS} = 50 V, V_{GS} = 10 V, I_D = 10 A, R_g = 3.3 Ω	t_f	-	1.4	-	ns
Body-Diode PARAMETERS					
Drain-Source Diode Forward Voltage at I_S = 1 A, V_{GS} = 0 V	V_{SD}	-	-	1	V
Body-Diode Continuous Current	I_S	-	-	17.8	A
Body-Diode Continuous Current, Pulsed	I_{SM}	-	-	45	A
Body Diode Reverse Recovery Time at I_S = 10 A, di/dt = 100 A / µs	t_{rr}	-	38	-	ns
Body Diode Reverse Recovery Charge at I_S = 10 A, di/dt = 100 A / µs	Q_{rr}	-	24	-	nC

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Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

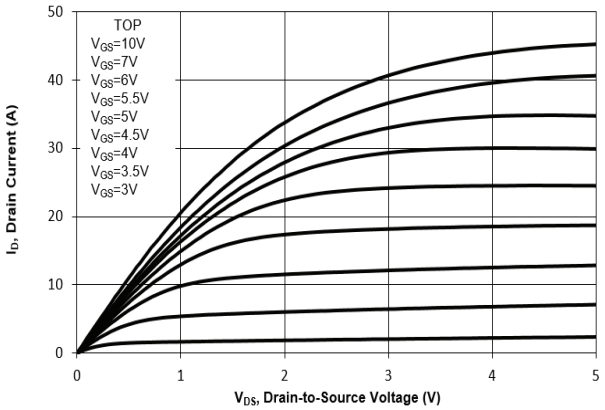


Fig. 2 Typical Transfer Characteristics

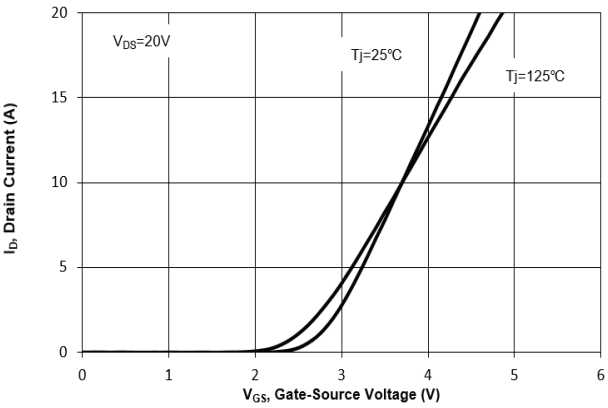


Fig. 3 On-Resistance vs. Drain Current

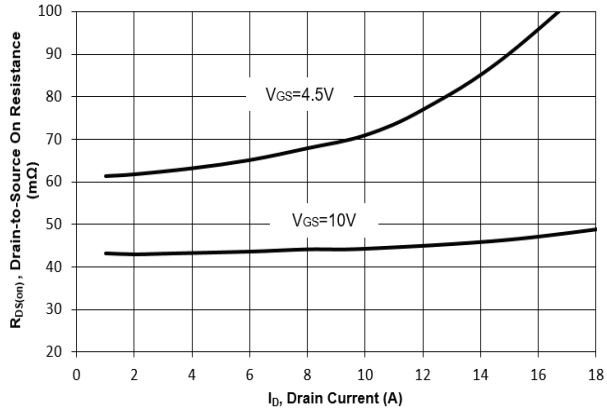


Fig. 4 On-Resistance vs. Gate to Source Voltage

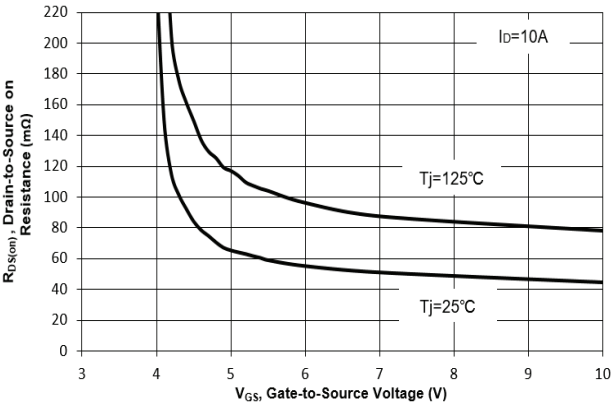


Fig. 5 On-Resistance vs.T_j

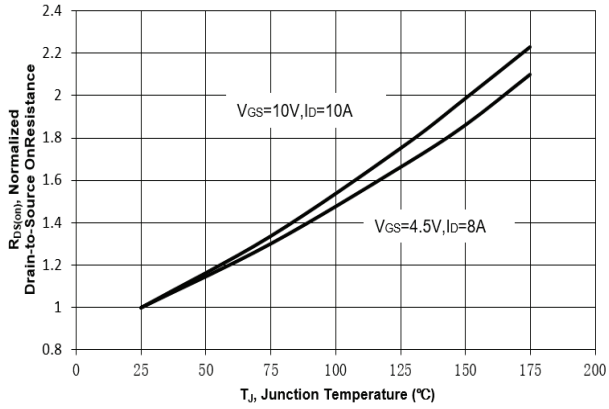
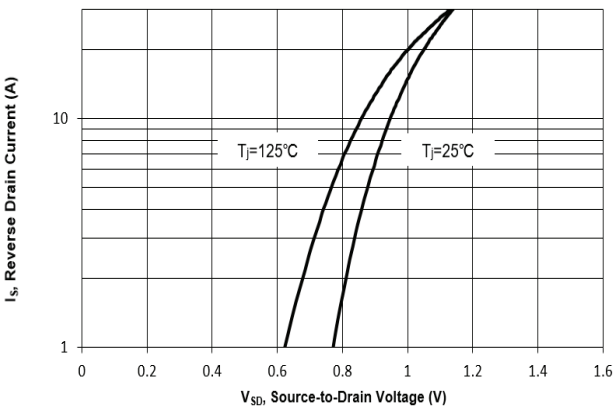


Fig. 6 Typical Body-Diode Forward Characteristics



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Electrical Characteristics Curves

Fig.13 Normalized Maximum Transient Thermal Impedance($z_{\theta JC}$)

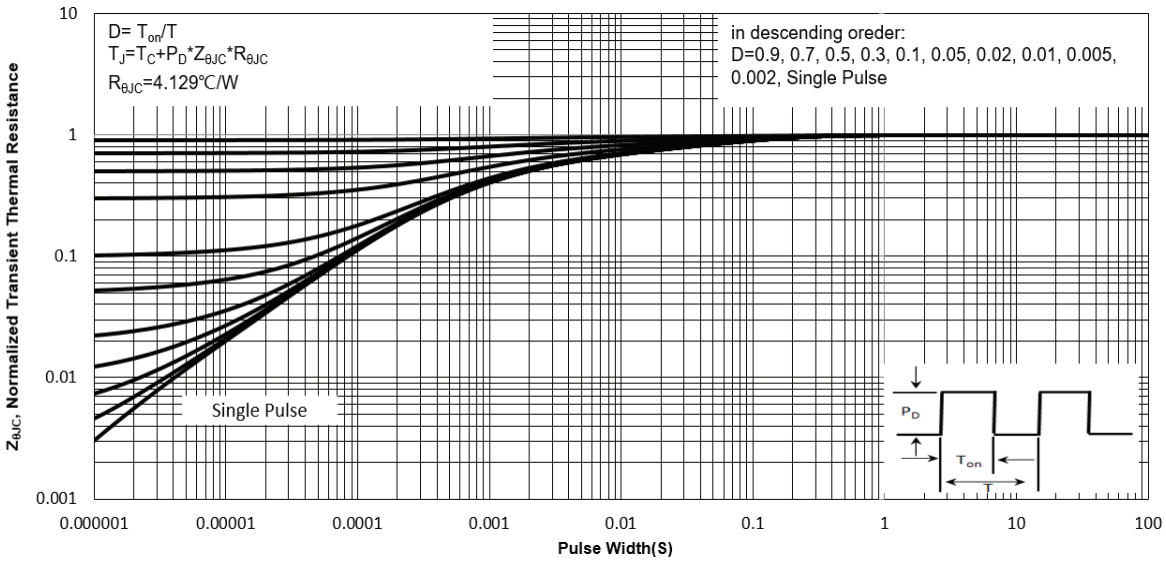

Fig.14 Normalized Maximum Transient Thermal Impedance($z_{\theta JA}$)

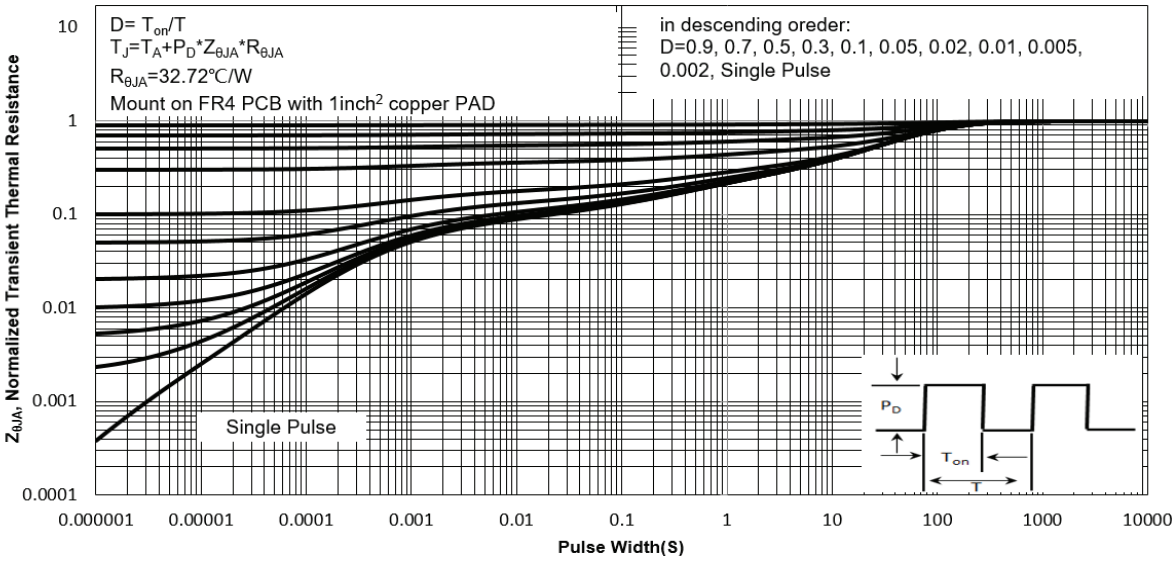

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Fig. 7 Typical Junction Capacitance

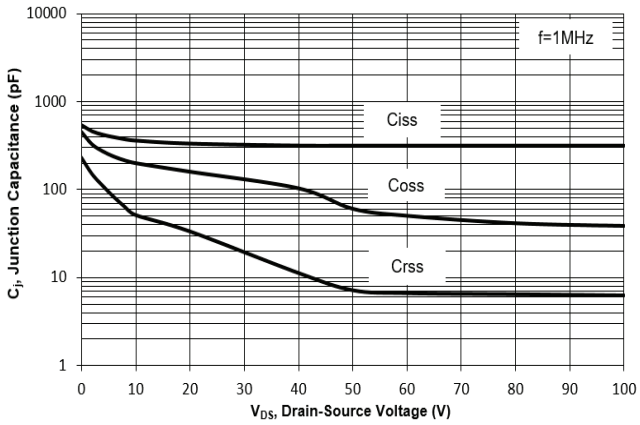


Fig. 8 Drain-Source Leakage Current vs. T_j

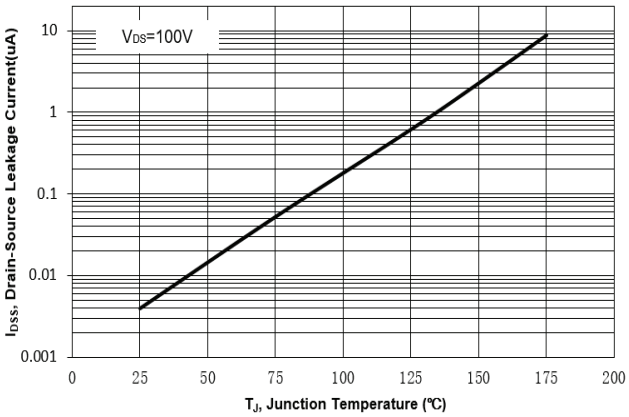


Fig. 9 $V_{(BR)DSS}$ vs. Junction Temperature

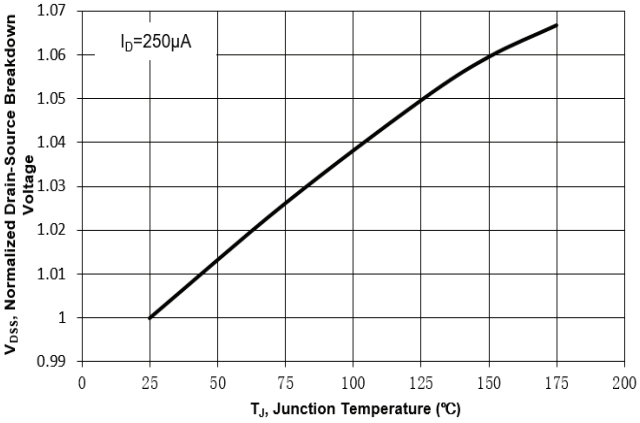


Fig. 10 Gate Threshold Variation vs. T_j

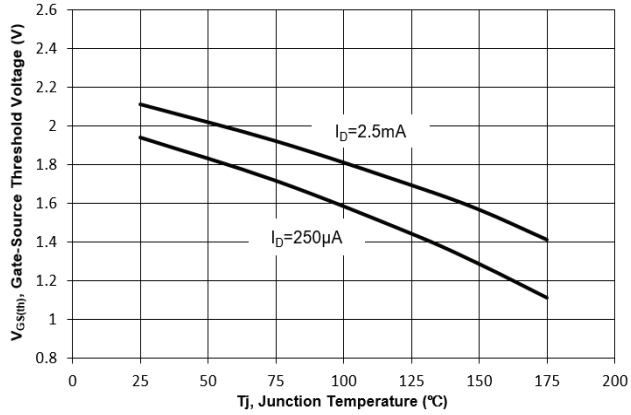


Fig. 11 Gate Charge

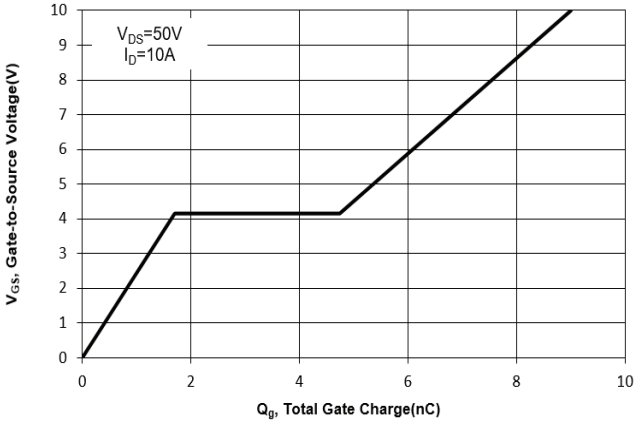
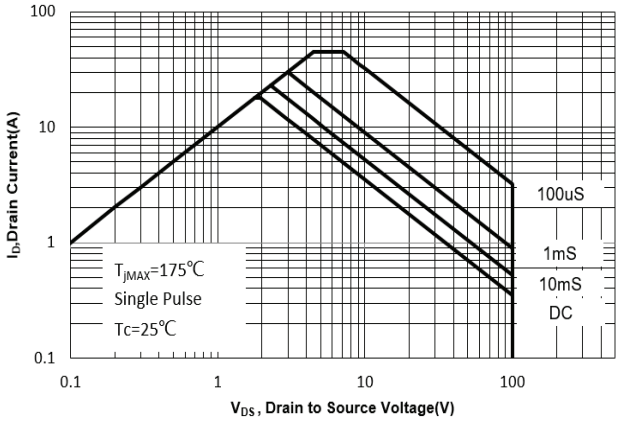


Fig. 12 Safe Operation Area



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Test Circuits

Fig.1-1 Switching times test circuit

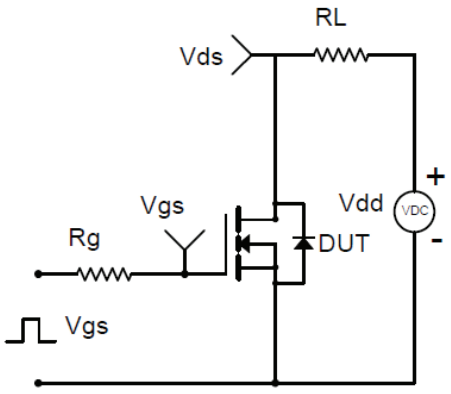


Fig.1-2 Switching Waveform

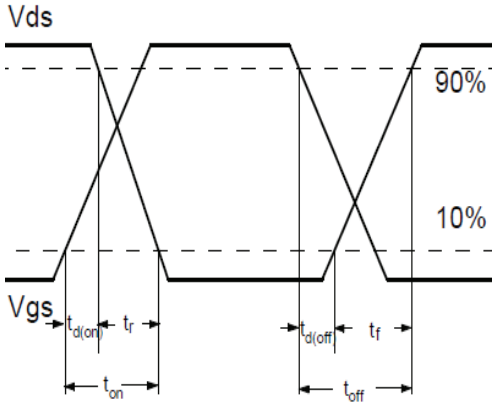


Fig.2-1 Gate charge test circuit

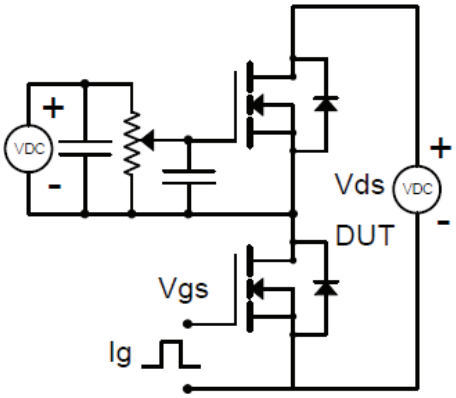


Fig.2-2 Gate charge waveform

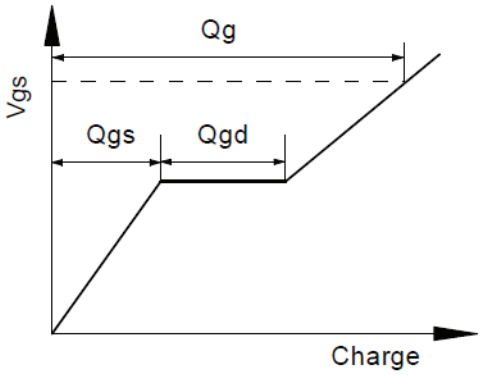


Fig.3-1 Avalanche test circuit

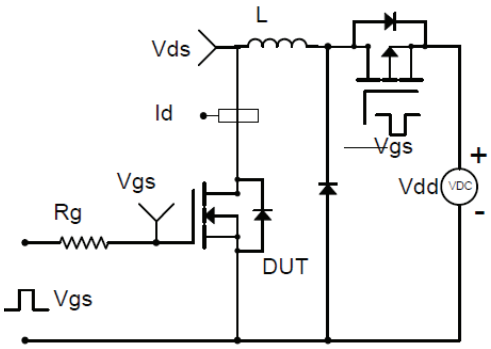
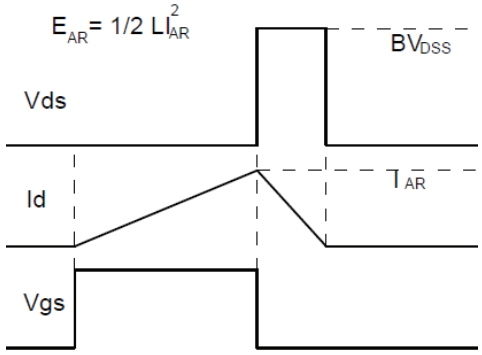


Fig.3-2 Avalanche waveform



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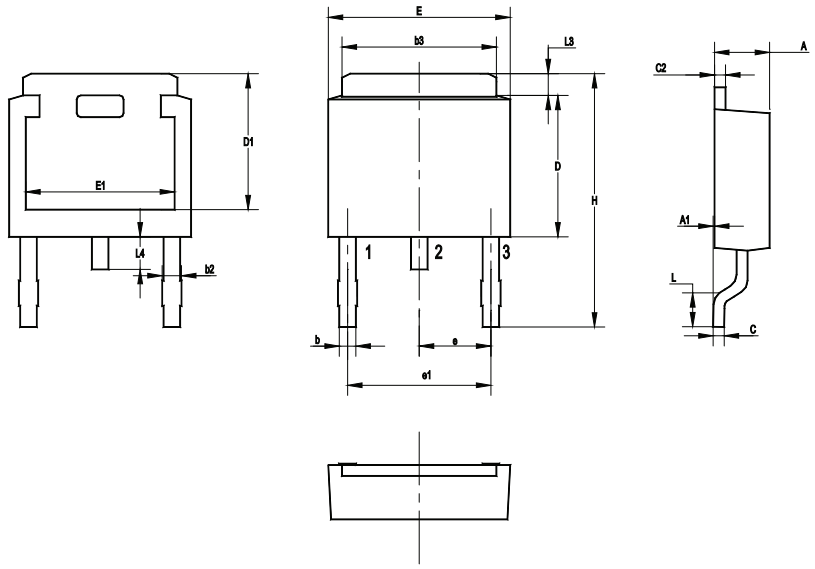
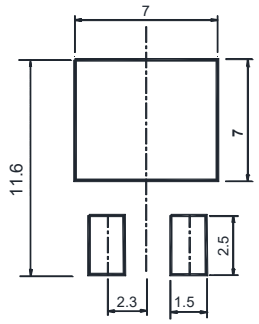
Package Outline (Dimensions in mm)

TO-252



UNIT	A	A1	b	b2	b3	C	C2	D	D1	E	E1	e	e1	H	L	L3	L4
mm	2.5	0.15	1.0	1.15	5.5	0.65	0.65	6.2	5.4	6.7	5.0	2.30	4.60	10.7	1.78	1.20	1.10
	2.1	0	0.5	0.65	4.9	0.4	0.4	5.6	5.0	6.1	4.6	TYP.	TYP.	9	1.40	0.85	0.51

Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
TO-252	16	8 ± 0.1	0.315 ± 0.004	330	13	2,500

Marking information

" DR10N680LK " = Part No.
" ****** " = Date Code Marking
Font type: Arial

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